1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,X1036

LAST_MODIFICATION=Thu Jul 12 17:54:35 2018

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0013100592	ENGINEERING RELEASED	2018-07-12

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DRAWING
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ABBREV=ABBREV
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Schematic / PCB /MCO #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02424	1	SCHEM,MLB,X1036	SCH	CRITICAL	
820-00939	1	PCBF,MLB,X1036	PCB	CRITICAL	
056-04386	1	MCO,MLB,X1036	MCO	CRITICAL	

Module Parts

TBT X,T

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00356	2	IC,TBT,TITAN RIDGE,QTZZ,ES2,B0,CSP337	U2800,UB000	CRITICAL	TBT_TR:B0
338S00408	2	IC,TBT,TITAN RIDGE,QUJK,QS,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1_QS
338S00441	2	IC,TBT,TITAN RIDGE,QUJK,PRQ,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1

ACE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S01442	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0_nFBGA
353S01478	4	IC,CD3215,ACE2,USB PWR SW,BLNK,BGA123	U3100,U3200,UB300,UB400	CRITICAL	ACE2:A0
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,jrBGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0

SOC PMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00342	1	IC,PMU,CALPE_L,D2249A0,OTP-AC,CSP324,0.5	U7800	CRITICAL	PMU:A0_C

SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00386	1	POP.SOC,GIBRALTAR+1G 21NM,M,Dev,CSP1122	U3900	CRITICAL	SOC:1G_DEV
339S00388	1	POP.SOC,GIBRALTAR+1G 21NM,M,Dev,CSP1122	U3900	CRITICAL	SOC:2G_DEV

10Gb ETHERNET CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00332	1	IC,ENET CONTROLLER,AQC107,B1,BGA224	U9600	CRITICAL	10G_ENET:B1

1Gb ETHERNET CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0616	1	IC,ENET CONTROLLER,CAESAR,A0	U9300	CRITICAL	1G_ENET:A0

WiFi/BT CONTROLLER (Should have alternatives)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00458	1	IC,MODULE,HARPOON,ES7.7,LGA385	U3730	CRITICAL	WIFI:ES7

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00428	339S00458		ALL	IC,MODULE,WCF2/BT,HARPOON,USI,ES7.5,LGA385

HDMI CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00347	1	PCON,MADEA,A4	UA800	CRITICAL	HDMI:A4

PoWER CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00928	1	IC,ISL95828A,IMVP0 CPU REG,QFN48,6x6mm	U7100	CRITICAL	

CPU

4C CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00457	1	CPU,CFL-H	U0500	CRITICAL	CPU:PES
337S00555	1	CPU,CFL-H,QQ5N,EQS,2.8GHz	U0500	CRITICAL	CPU_EQS:2.8G
337S00554	1	CPU,CFL-H,QQ5K,EQS,3.0GHz	U0500	CRITICAL	CPU_EQS:3.0G
337S00553	1	CPU,CFL-H,QQ5C,EQS,3.2GHz	U0500	CRITICAL	CPU_EQS:3.2G
998-12472	1	INTERPOSER,,CFL-H, BGA1440	U0500	CRITICAL	CPU:SOCKET
337S00570	1	CPU,CFL-H,SRCX4,PRQ,2.8GHz	U0500	CRITICAL	CPU:2.8G
337S00569	1	CPU,CFL-H,SRCX3,PRQ,3.0GHz	U0500	CRITICAL	CPU:3.0G
337S00568	1	CPU,CFL-H,SRCX2,PRQ,3.2GHz	U0500	CRITICAL	CPU:3.2G
337S00618	1	CPU,CFL-H,SRDEC,PRQ,3.6GHz	U0500	CRITICAL	CPU:3.6G

PCH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00470	1	PCH-H,CNL,QNDQ,ES,A1,BGA874	U1200	CRITICAL	PCH:ES
337S00536	1	PCH-H,CNL,QNYJ,QS,B0,BGA874	U1200	CRITICAL	PCH:QS
337S00577	1	PCH-H,CNL,QNYJ,PRQ,B0,BGA874	U1200	CRITICAL	PCH:PRQ

SSD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-12416	4	NAND,3DV3,42GBP,S4E,170G,T,SUB X,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:128_TB
998-12418	4	NAND,3DV3,85GBP,S4E,170G,T,SUB X,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:256_TB
998-12420	4	NAND,3DV3,128GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:512_TB
998-12424	4	NAND,3DV3,256GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_TB
335S00323	4	NAND,3DV3,42GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:128_SD
335S00324	4	NAND,3DV3,85GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:256_SD
335S00325	4	NAND,3DV3,128GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:512_SD
335S00327	4	NAND,3DV3,256GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_SD
335S00321	4	NAND,3DV4,256GB,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_SM
335S00373	4	NAND,3DV4,512GB,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:2T_SM

<- new DVT

SSD ALTERNATIVES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
998-12421	998-12420	ALL	SSD:512 TB W/X	SSD:512_TB

998-12416 SSD:128_TB_X or TB1
998-12417 SSD:128_TB_W or TB2 TB2 dropped per Marketing

998-12418 SSD:256_TB_X or TB1
998-12419 SSD:256_TB_W or TB2 TB2 dropped per Marketing

998-12420 SSD:512_TB_X or TB1
998-12421 SSD:512_TB_W or TB2

998-12424 SSD:1T_TB_X or TB1
998-12426 SSD:1T_TB_W or TB2 TB2 dropped per Marketing

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Programmable Parts

TBT X ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	TBT_X_ROM:BLANK
341S00987	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:POC
341S00987	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:PROTO
341S01094	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:PREEVT
341S01111	1	IC,T29,TBT-X,R1,V21.3,EXT,X1036	U2890	CRITICAL	TBT_X_ROM:EVT
341S01171	1	IC,T29,TBT-X,R1,V28.1,DXT,X1036	U2890	CRITICAL	TBT_X_ROM:DVT

TBT T ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UB090	CRITICAL	TBT_T_ROM:BLANK
341S00988	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:POC
341S00988	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:PROTO
341S01095	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:PREEVT
341S01110	1	IC,T29,TBT-T,R0,V21.3,EVT,X1036	UB090	CRITICAL	TBT_T_ROM:EVT
341S01170	1	IC,T29,TBT-T,R0,V28.1,DVT,X1036	UB090	CRITICAL	TBT_T_ROM:DVT

MADEA(HDMI) SPI ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00049	1	MADEA SPI FLASH,8MB,1.8V,8P,USON	UA801	CRITICAL	HDMI_ROM:BLANK
341S00991	1	IC,HDMI(V1.106),DEV,X1036	UA801	CRITICAL	HDMI_ROM:PROTO
341S01096	1	IC,HDMI(V1.106),DEV,X1036	UA801	CRITICAL	HDMI_ROM:PREEVT
341S01112	1	IC,HDMI(V2.245),EVT,X1036	UA801	CRITICAL	HDMI_ROM:EVT
341S01172	1	IC,HDMI(V2.005),DVT,X1036	UA801	CRITICAL	HDMI_ROM:DVT

10G ETHERNET ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00269	1	IC SPI FLASH,32MBIT,3V,SOIC8	U9890	CRITICAL	10G_ENET_ROM:BLANK
341S00989	1	IC,ETHERNET 10GB (V2.9.15) DEV,X1036	U9890	CRITICAL	10G_ENET_ROM:PROTO
341S01045	1	IC,ETHERNET 10GB (V2.9.15) DEV,X1036	U9890	CRITICAL	10G_ENET_ROM:PREEVT
341S01113	1	IC,ETHERNET 10GB (V2.10.1) EVT,X1036	U9890	CRITICAL	10G_ENET_ROM:EVT
341S01173	1	IC,ETHERNET 10GB (V2.10.8) DVT,X1036	U9890	CRITICAL	10G_ENET_ROM:DVT

1G ETHERNET ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV E,SOIC-8	U9390	CRITICAL	1G_ENET_ROM:BLANK
341S00990	1	IC,ETHERNET 1GB (V1.15) DEV,X1036	U9390	CRITICAL	1G_ENET_ROM:PROTO
341S01174	1	IC,ETHERNET 1GB (V1.15) DVT,X1036	U9390	CRITICAL	1G_ENET_ROM:DVT

BT SERIAL FLASH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00256	1	IC,SPI SERIAL FLASH,2MBIT,1.8V,DFN8	U3750	CRITICAL	BT_FLASH:BLANK
341S00965	1	BT SFLASH ROM(V21) PROTO-2,X1036	U3750	CRITICAL	BT_FLASH:POC
341S01025	1	BT SFLASH ROM(V32) proto,X1036	U3750	CRITICAL	BT_FLASH:PROTO
341S01098	1	BT SFLASH ROM(V32) preEVT,X1036	U3750	CRITICAL	BT_FLASH:PREEVT
341S01119	1	IC,BT SFLASH ROM(V45),EVT,X1036	U3750	CRITICAL	BT_FLASH:EVT
341S01175	1	IC,BT SFLASH ROM(V56),DVT,X1036	U3750	CRITICAL	BT_FLASH:DVT

WLAN SERIAL EEPROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00214	1	IC,EEPROM,SER,UWIRE,16K,1.8V,DFN8	U3710	CRITICAL	WLAN_EEPROM:BLANK
341S00725	1	WIFI ROM,V01,WW1,X665	U3710	CRITICAL	WLAN_EEPROM:DVT

The same as proto and later

SOC ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SPI,4MX8.1V8,DFN8	U4770	CRITICAL	SOC_ROM:BLANK

SEP EEPROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00469	1	IC,MCU,ARM,SC000,STLNX,A0,DIVKEY,DFN8	U4730	CRITICAL	SEPROM:LYNX
335S0888	1	IC,SERIAL I2C EEPROM,128KBIT,8P,MLP6	U4730	CRITICAL	SEPROM:OG

Alternatives section 1

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
152S00573	152S1778	ALL	INDUCTOR	
152S00748	152S00697	ALL	INDUCTOR	
152S00801	152S00695	ALL	INDUCTOR	
155S00363	155S00364	ALL	CMC	
353S00772	353S4070	ALL	DISPLAY MUX	
353S4068	353S4070	ALL	DISPLAY MUX	
376S00074	376S0855	ALL	DUAL FET	
372S0186	372S0185	ALL	TRANSISTOR	
371S00095	371S0567	ALL	DIODE	
371S0684	371S0495	ALL	DIODE	
371S00042	371S00125	ALL	DIODE	
339S00389	339S00388	ALL	H9ML	
311S00013	311S0508	ALL	BUFFER	
335S00270	335S00203	ALL	SoC ROM	
128S00081	128S0264	ALL	CAP	
128S0364	128S0264	ALL	CAP	
377S0155	377S0184	ALL	ESD Diode	
377S0077	377S0183	ALL	ESD Diode	
377S00079	377S00077	ALL	Diode	
377S0178	377S00031	ALL	ESD Diode	
376S00224	376S1128	ALL	FET	
353S01041	353S01042	ALL	Vref IC	
353S00750	353S00877	ALL	LDO	
376S0636	376S1004	ALL	FET	
311S0426	311S00007	ALL	BUFFER	
335S00213	335S0888	ALL	SEP ROM	
311S0596	311S0593	ALL	LOGIC GATE	
311S0372	311S0562	ALL	LOGIC GATE	
311S00138	311S0436	ALL	LEVEL SHIFTER	
311S0562	311S0372	ALL	LOGIC GATE	
311S00133	311S00130	ALL	BUFFER	
197S00118	197S00120	ALL	CRYSTAL	
197S0612	197S00120	ALL	CRYSTAL	
197S00053	197S00050	ALL	Y1900 radar 37073234	
197S00054	197S00050	ALL	Y1900 radar 37073234	
197S00055	197S00050	ALL	Y1900 radar 37073234	
197S00048	197S00036	ALL	Y3800,etc radar 37073152	
311S00121	311S0398	ALL	AND Gate DFN pack	
311S0398	311S00121	ALL	AND Gate DFN pack	
138S0860	138S0775	ALL	C7101,etc radar 38188751	
138S0933	138S0931	ALL	C7525,etc radar 38079576	

Alternatives section continued on CSA 142

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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SHEET: 3 OF 115

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Boss on TOP side

2x 860-00935.

B0400
8.70D4.2ID-1.75H-SM

B0401
8.70D4.2ID-1.75H-SM

9x 860-00913.

B0406
BOSS-3.00D1.20ID-2.80H-SM

B0409
BOSS-3.00D1.20ID-2.80H-SM

B0410
BOSS-3.00D1.20ID-2.80H-SM

B0412
BOSS-3.00D1.20ID-2.80H-SM

B0413
BOSS-3.00D1.20ID-2.80H-SM

B0414
BOSS-3.00D1.20ID-2.80H-SM

B0415
BOSS-3.00D1.20ID-2.80H-SM

B0417
BOSS-3.00D1.20ID-2.80H-SM

B0416
BOSS-3.00D1.20ID-2.80H-SM

Boss on BOTTOM side

2x 860-00929.

B0407
BOSS-6.00D5.95H-TH-1.4-2.6

B0418
BOSS-6.00D5.95H-TH-1.4-2.6

2x 860-1438.

B0404
4.00D1.55H-M1.6X0.35-ST

B0403
4.00D1.55H-M1.6X0.35-ST
WIFI

2x 860-01020.

B0419
BOSS-4.00D2.2ID-4.25H-SM

B0408
BOSS-4.00D2.2ID-4.25H-SM

CPU Sled on TOP side:

2x 806-16518

CKPLUS_WAIVE=TERMSHORTED
SP0400
SLED-CPU-X1035
SMT-PAD-SP

CKPLUS_WAIVE=TERMSHORTED
SP0401
SLED-CPU-X1035
SMT-PAD-SP

Antenna cable clips:

3x 806-15581.

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0400
SM

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0401
SM

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0402
SM

Shield Cans:

604-19182.DIMM Shield
SH0400
SM
SHLD-FENCE-DIMM-X1035

806-14422.H9ML Fence
SH0401
SM
SHLD-FENCE-GIB-X1035

806-14495.Harpoon Fence
SH0402
SM
SHLD-FENCE-HARPN-X1035

806-16657 HDMI Shield Can
SH0420
SM
SHLD-HDMI-X1035

806-14019.UBSC-IO EMI Fence
SH0404
SM
SHLD-FENCE-TOP-USBC-X1035

806-14020.IO EMI Fence
SH0407
SM
SHLD-FENCE-TOP-IO-X1035

806-14423.Ridge Shield
SH0405
SM
SHLD-FENCE-RIDGE-X1035

806-14022 SSD Fence
SH0406
SM
SHLD-FENCE-SSD-X1035

806-15424.Diplexer Shield Can
SH0408
SM
SHLD-MLB-DIPLEXERS-X1035

Through holes of shields:

DIMM shield holes:2x 998-13324

SL0411
TH-NSP
SL-1.5X0.55-1.9X0.95

SL0413
TH-NSP
SL-1.5X0.55-1.9X0.95

Harpoon shield holes:2x 998-04440

SL0400
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0401
TH-NSP
SL-1.2X0.4-1.5X0.7

USBC IO shield holes:2x 998-04440

SL0403
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0402
TH-NSP
SL-1.2X0.4-1.5X0.7

3-pack IO shield holes:1x 998-04440
1x 998-13325

SL0404
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0412
TH-NSP
SL-1.05X0.4-1.45X0.8

Ridges shield holes:2x 998-04440

SL0406
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0405
TH-NSP
SL-1.2X0.4-1.5X0.7

H9ML shield holes:2x 998-04440

SL0408
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0407
TH-NSP
SL-1.2X0.4-1.5X0.7

SSD shield holes:2x 998-04440

SL0410
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0409
TH-NSP
SL-1.2X0.4-1.5X0.7

HDMI shield holes:2x 998-04440

SL0420
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0421
TH-NSP
SL-1.2X0.4-1.5X0.7

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=Mary
SYNC_DATE=04/26/2018

PAGE TITLE
PD Parts

Apple Inc.

DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
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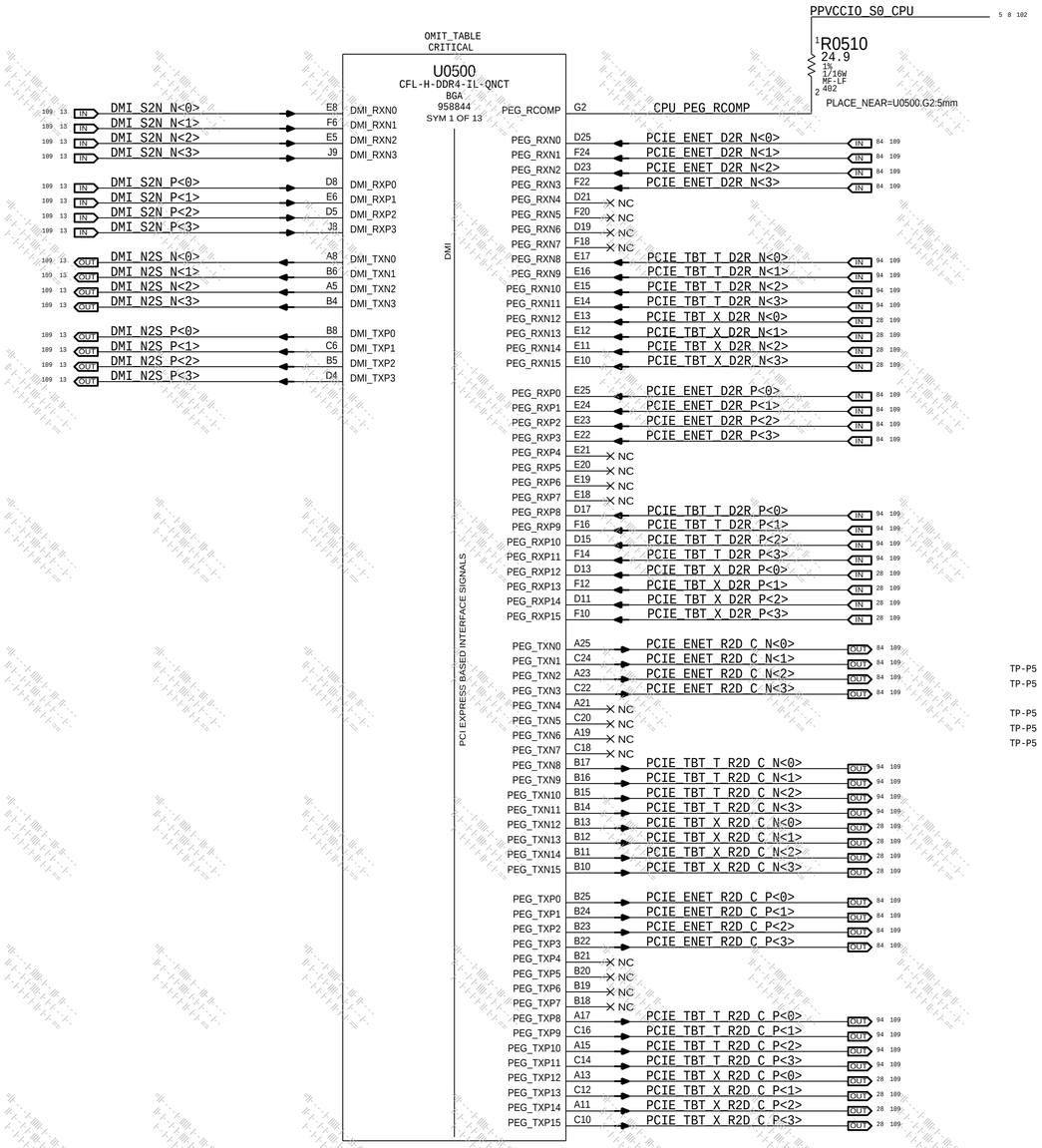

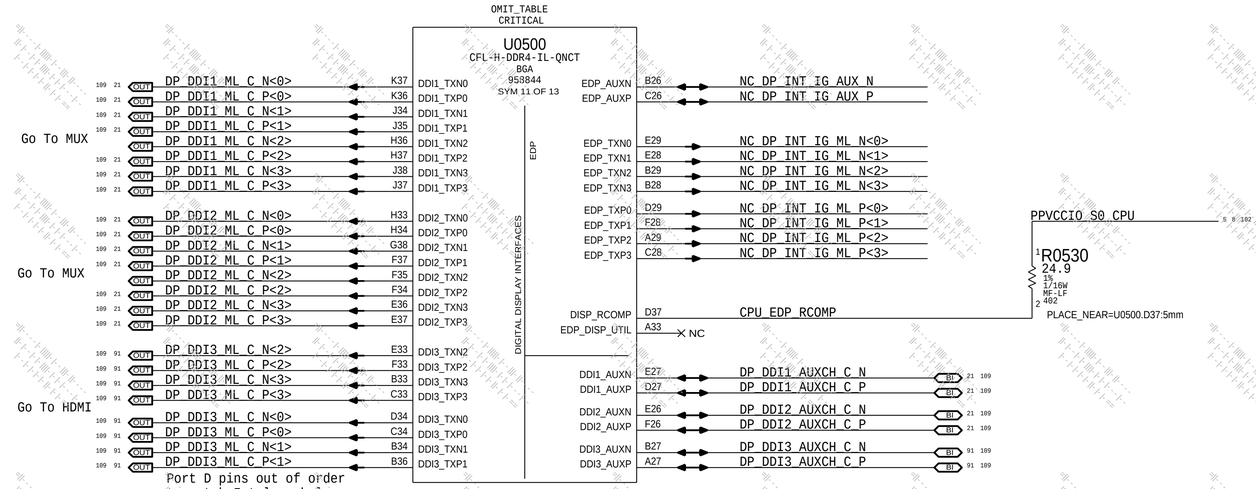

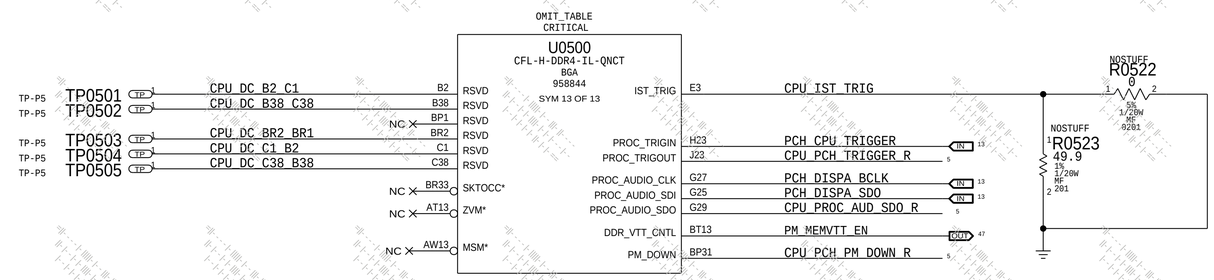

CPU Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	CPU DMI/PEG/FDI/RSVD
Apple Inc.	DRAWING NUMBER 051-02424 · SIZE D
	REVISION 6.0.0
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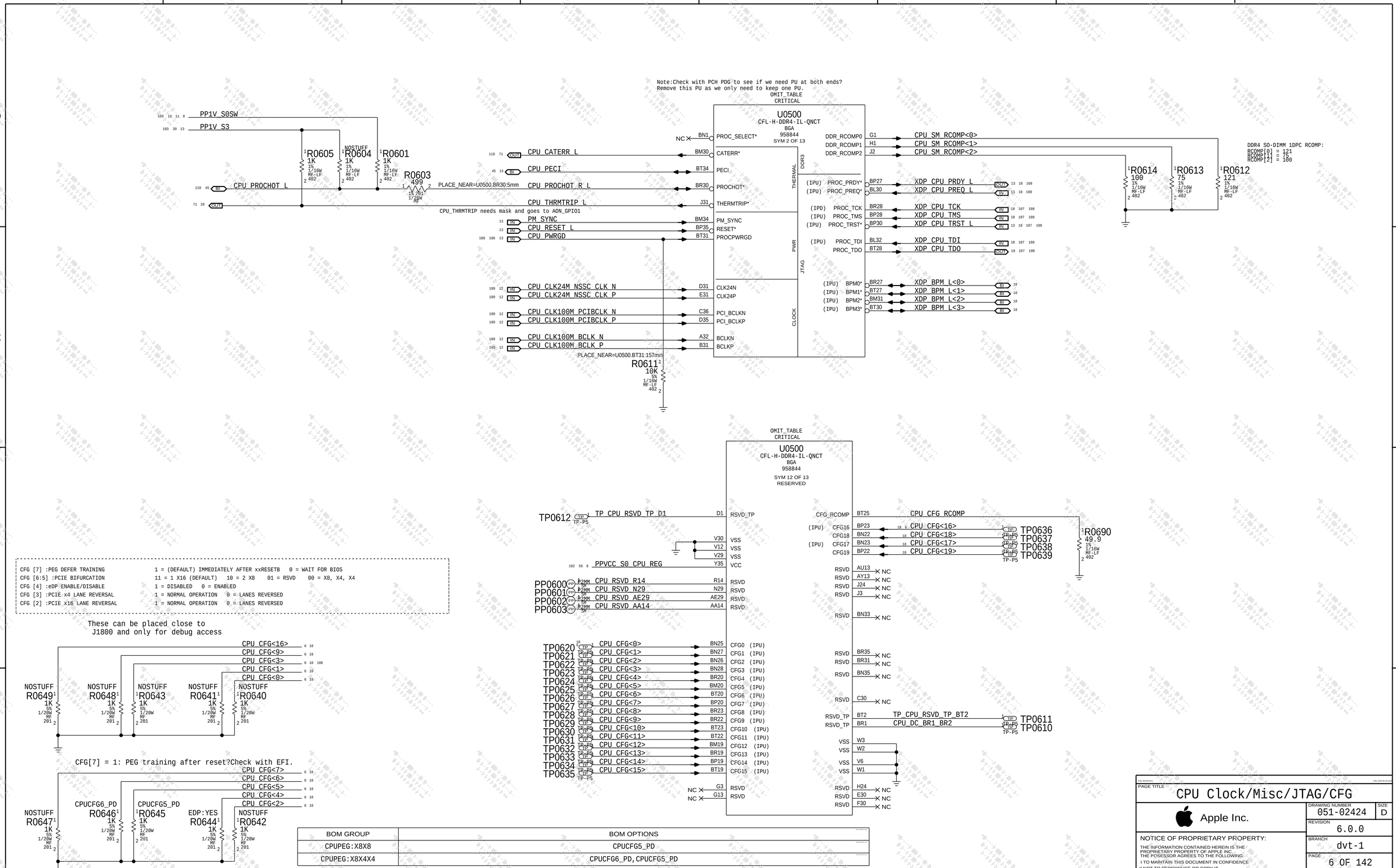
	PAGE 5 OF 142
	SHEET 5 OF 115


Note:Check with PCH PDG to see if we need PU at both ends?
Remove this PU as we only need to keep one PU.
OMIT_TABLE
CRITICAL
U0500
CFL-H-DDR4-IL-QNCT
BGA
958844
SYM 2 OF 13
PP1V S0SW
PP1V S3
R0605 1K
NOSTUFF R0604 1K
R0601 1K
R0603 499
CPU PROCHOT L
CPU CATERR L
CPU PECI
PLACE_NEAR=U0500.BR30:5mm
CPU PROCHOT R L
CPU THRMTRIP L
CPU_THRMTRIP needs mask and goes to AON_GPIO1
PM SYNC
CPU RESET L
CPU PWRGD
CPU CLK24M NSSC CLK N
CPU CLK24M NSSC CLK P
CPU CLK100M PCIBCLK N
CPU CLK100M PCIBCLK P
CPU CLK100M BCLK N
CPU CLK100M BCLK P
PLACE_NEAR=U0500.BT31:157mil
R0611 10K
NC
PROC_SELECT*
CATERR*
PECI
PROCHOT*
THERMTRIP*
PM_SYNC
RESET*
PROCPWRGD
CLK24N
CLK24P
PCI_BCLKN
PCI_BCLKP
BCLKN
BCLKP
THERMAL
DDR3
PWR
JTAG
CLOCK
DDR_RCOMP0
DDR_RCOMP1
DDR_RCOMP2
CPU SM RCOMP<0>
CPU SM RCOMP<1>
CPU SM RCOMP<2>
XDP CPU PRDY L
XDP CPU PREQ L
XDP CPU TCK
XDP CPU TMS
XDP CPU TRST L
XDP CPU TDI
XDP CPU TDO
XDP BPM L<0>
XDP BPM L<1>
XDP BPM L<2>
XDP BPM L<3>
R0614 100
R0613 75
R0612 121
DDR4 SO-DIMM 1DPC RCOMP:
RCOMP[0] = 121
RCOMP[1] = 75
RCOMP[2] = 100
OMIT_TABLE
CRITICAL
U0500
CFL-H-DDR4-IL-QNCT
BGA
958844
SYM 12 OF 13
RESERVED
TP0612 TP CPU RSVD TP D1
PPVCC_S0_CPU_REG
PP0600 CPU RSVD R14
PP0601 CPU RSVD N29
PP0602 CPU RSVD AE29
PP0603 CPU RSVD AA14
TP0620 CPU_CFG<0>
TP0621 CPU_CFG<1>
TP0622 CPU_CFG<2>
TP0623 CPU_CFG<3>
TP0624 CPU_CFG<4>
TP0625 CPU_CFG<5>
TP0626 CPU_CFG<6>
TP0627 CPU_CFG<7>
TP0628 CPU_CFG<8>
TP0629 CPU_CFG<9>
TP0630 CPU_CFG<10>
TP0631 CPU_CFG<11>
TP0632 CPU_CFG<12>
TP0633 CPU_CFG<13>
TP0634 CPU_CFG<14>
TP0635 CPU_CFG<15>
CFG_RCOMP
CPU_CFG_RCOMP
CPU_CFG<16>
CPU_CFG<18>
CPU_CFG<17>
CPU_CFG<19>
TP0636
TP0637
TP0638
TP0639
R0690 49.9
TP_CPU_RSVD_TP_BT2
CPU_DC_BR1_BR2
TP0611
TP0610
CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
These can be placed close to
J1800 and only for debug access
NOSTUFF R0649 1K
NOSTUFF R0648 1K
NOSTUFF R0643 1K
NOSTUFF R0641 1K
NOSTUFF R0640 1K
CFG[7] = 1: PEG training after reset?Check with EFI.
NOSTUFF R0647 1K
CPUCFG6_PD R0646 1K
CPUCFG5_PD R0645 1K
EDP:YES R0644 1K
NOSTUFF R0642 1K
BOM GROUP
BOM OPTIONS
CPUPEG:X8X8
CPUCFG5_PD
CPUPEG:X8X4X4
CPUCFG6_PD,CPUCFG5_PD
To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CPU Clock/Misc/JTAG/CFG
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
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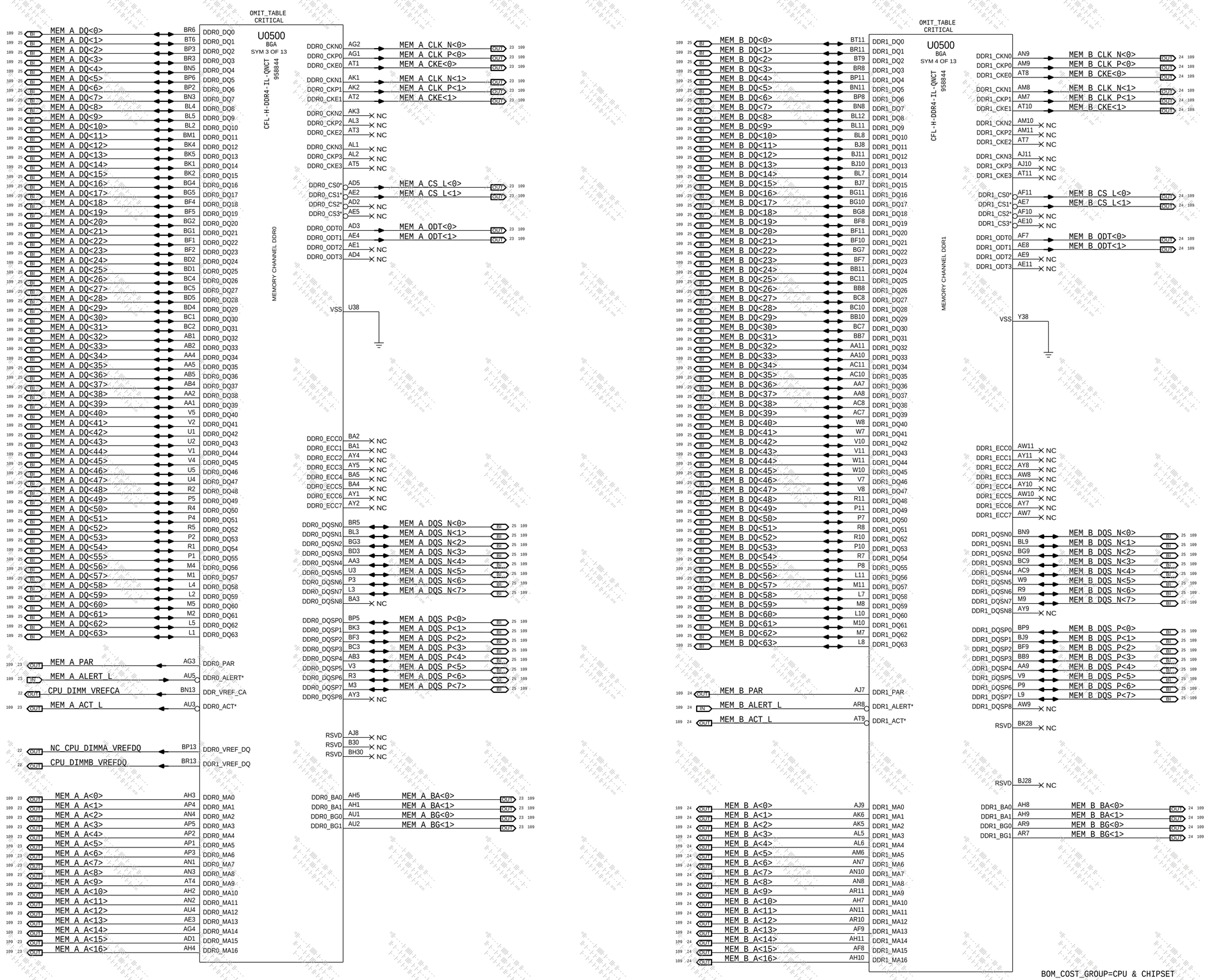

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=N/A SYNC_DATE=04/26/2016

PAGE TITLE

CPU DDR4 Interfaces

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

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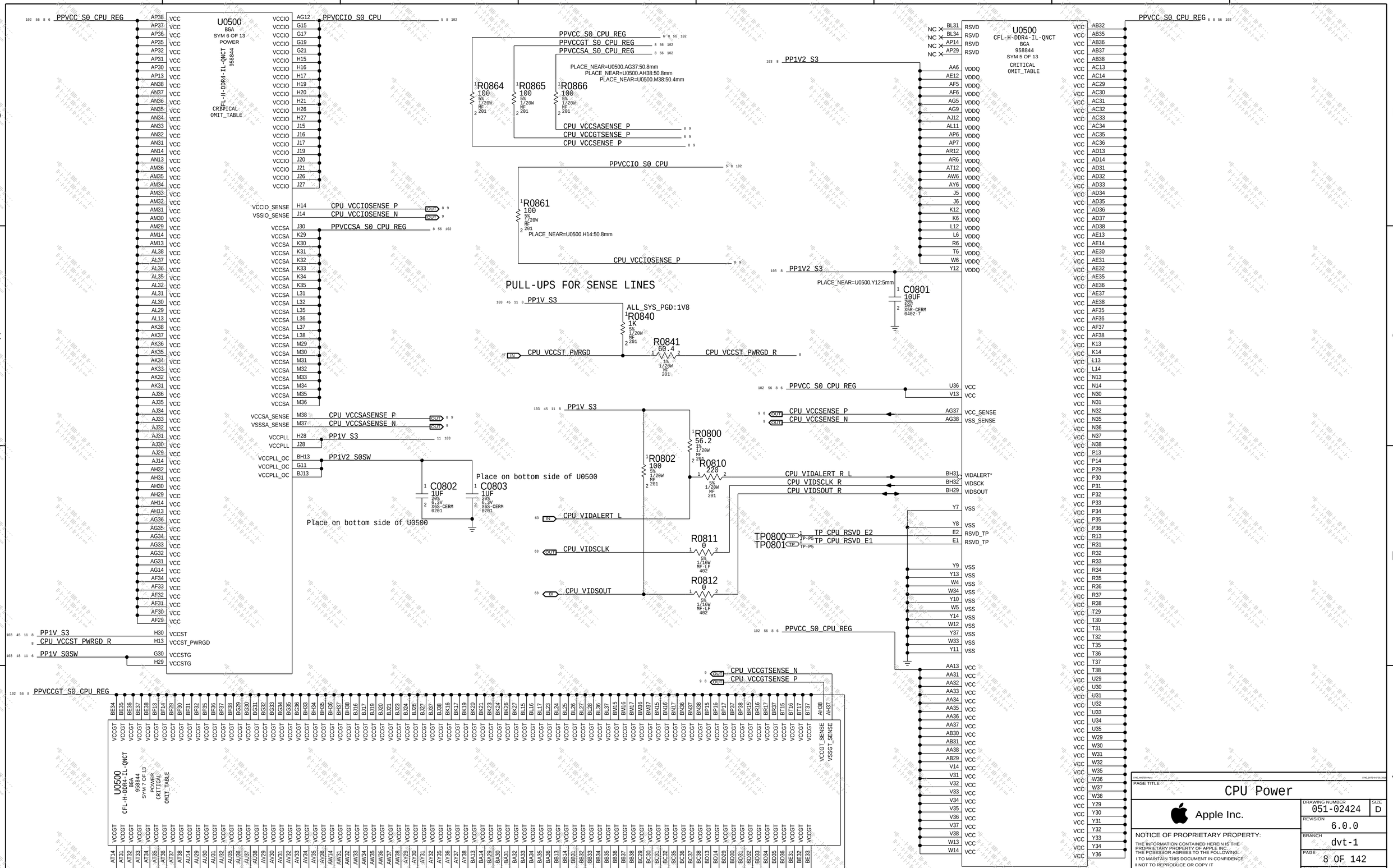
U0500
CFL-H-DDR4-IL-QNCT
BGA
SYM 6 OF 13
POWER
958844
CRITICAL
OMIT_TABLE
PPVCC_S0_CPU_REG
PPVCCIO_S0_CPU
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N
PPVCCSA_S0_CPU_REG
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
PP1V_S3
PP1V2_S0SW
C0802
1UF
20%
6.3V
X6S-CERM
0201
C0803
1UF
20%
6.3V
X6S-CERM
0201
Place on bottom side of U0500
Place on bottom side of U0500
PPVCC_S0_CPU_REG
PPVCCGT_S0_CPU_REG
PPVCCSA_S0_CPU_REG
R0864
100
5%
1/20W
MF
201
R0865
100
5%
1/20W
MF
201
R0866
100
5%
1/20W
MF
201
PLACE_NEAR=U0500.AG37:50.8mm
PLACE_NEAR=U0500.AH38:50.8mm
PLACE_NEAR=U0500.M38:50.4mm
CPU_VCCSASENSE_P
CPU_VCCGTSENSE_P
CPU_VCCSENSE_P
PPVCCIO_S0_CPU
R0861
100
5%
1/20W
MF
201
PLACE_NEAR=U0500.H14:50.8mm
CPU_VCCIOSENSE_P
PULL-UPS FOR SENSE LINES
PP1V_S3
ALL_SYS_PGD:1V8
R0840
1K
5%
1/20W
MF
201
R0841
60.4
1%
1/20W
MF
201
CPU_VCCST_PWRGD
CPU_VCCST_PWRGD_R
R0800
56.2
1%
1/20W
MF
201
R0802
100
5%
1/20W
MF
201
R0810
220
5%
1/20W
MF
201
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0811
0
5%
1/10W
MF-LF
402
R0812
0
5%
1/10W
MF-LF
402
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
TP0800
TP0801
TP_CPU_RSVD_E2
TP_CPU_RSVD_E1
PP1V2_S3
PLACE_NEAR=U0500.Y12:5mm
C0801
10UF
20%
10V
X5R-CERM
0402-7
PPVCC_S0_CPU_REG
CPU_VCCSENSE_P
CPU_VCCSENSE_N
PP1V2_S3
PP1V_S3
CPU_VCCST_PWRGD_R
PP1V_S0SW
PPVCCGT_S0_CPU_REG
CPU_VCCGTSENSE_N
CPU_VCCGTSENSE_P
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CPU Power
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
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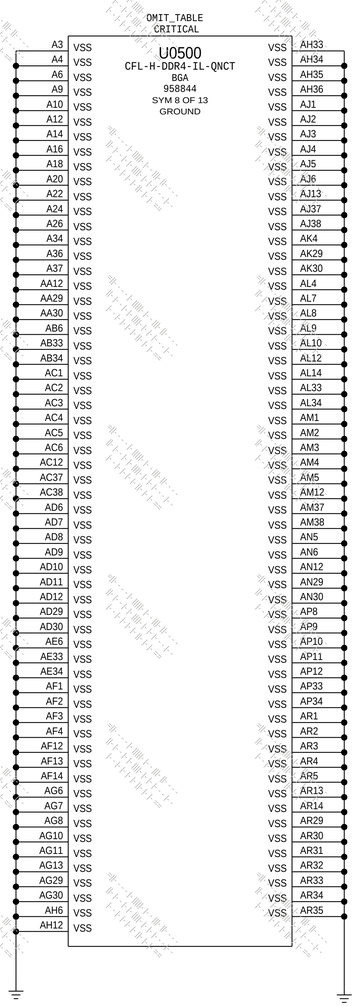

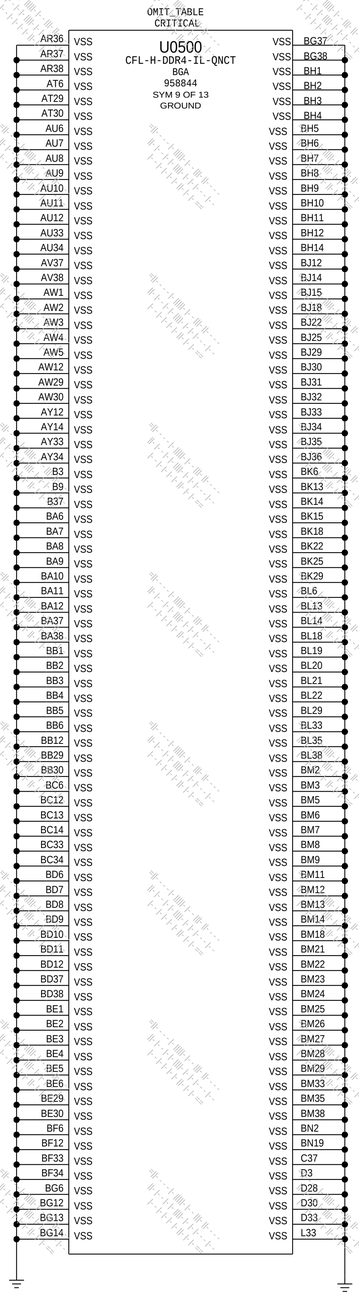

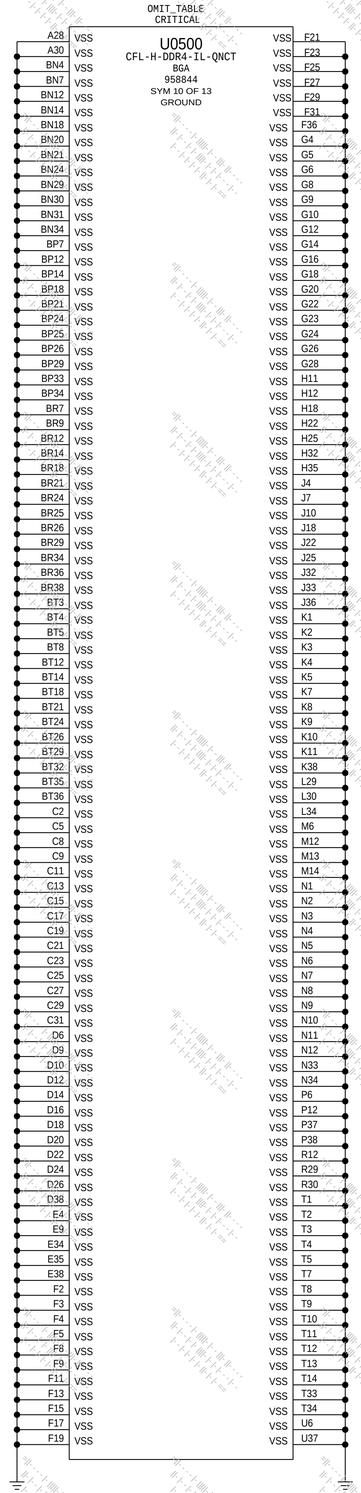

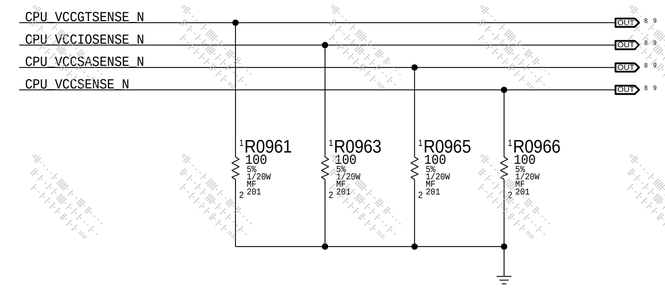

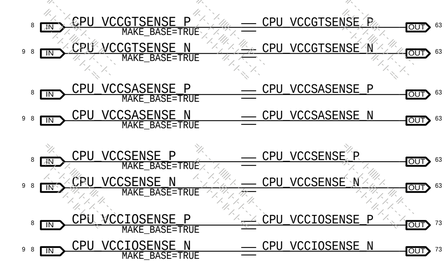

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

CPU Ground

Apple Inc.

DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

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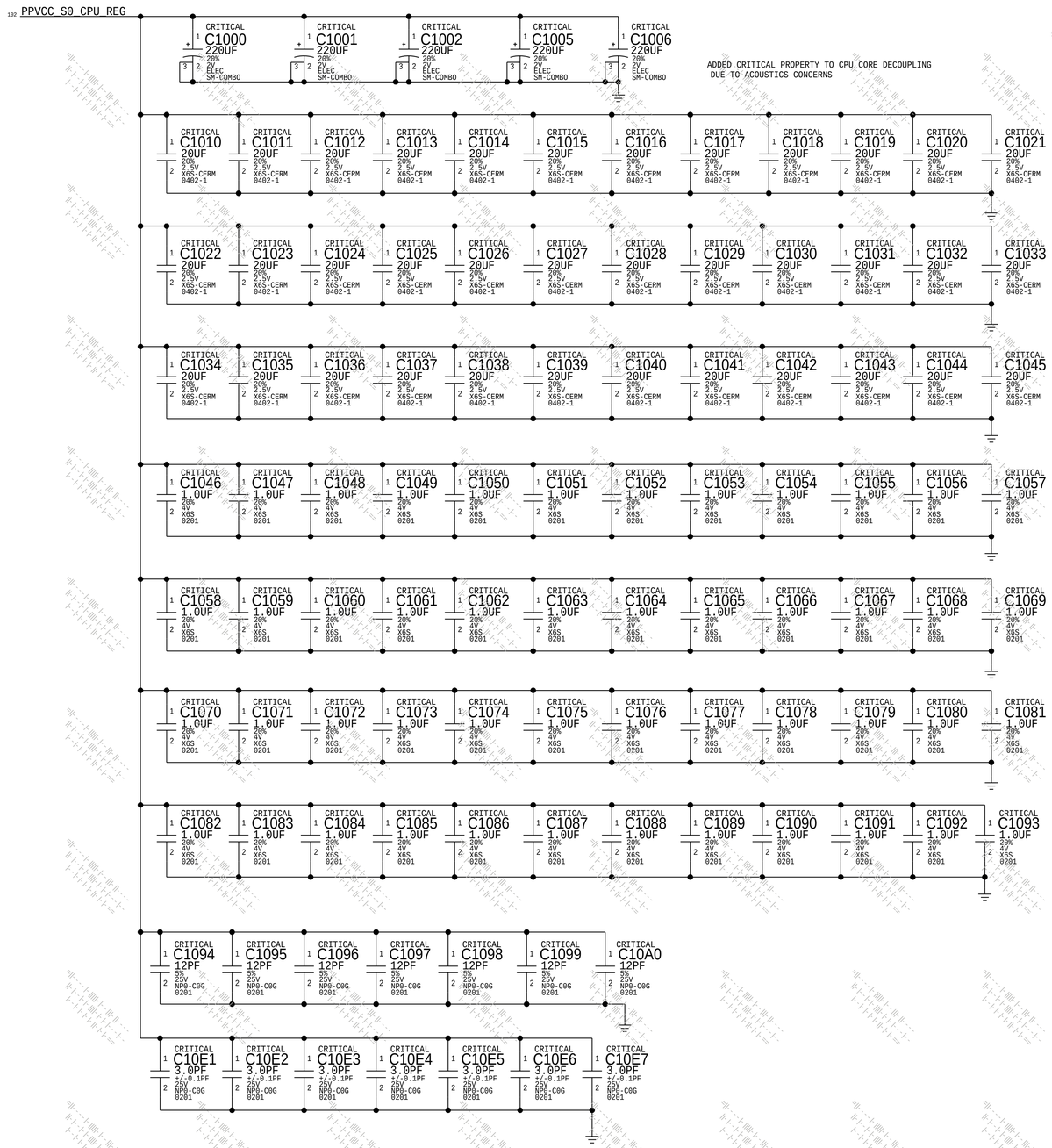
CPU VCORE DECOUPLING

Intel Recommendation:3x 330uF near CPU
5x 47uF 0805 @ board edge
12x 22UF 0603,21x 10uF 0402,24x 1uF 0201,24x 0201(placeholder) @ back side

Apple Implementation:5x 220uF
36x 20uF
48x 1uF
7x 12pF and 3pF

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



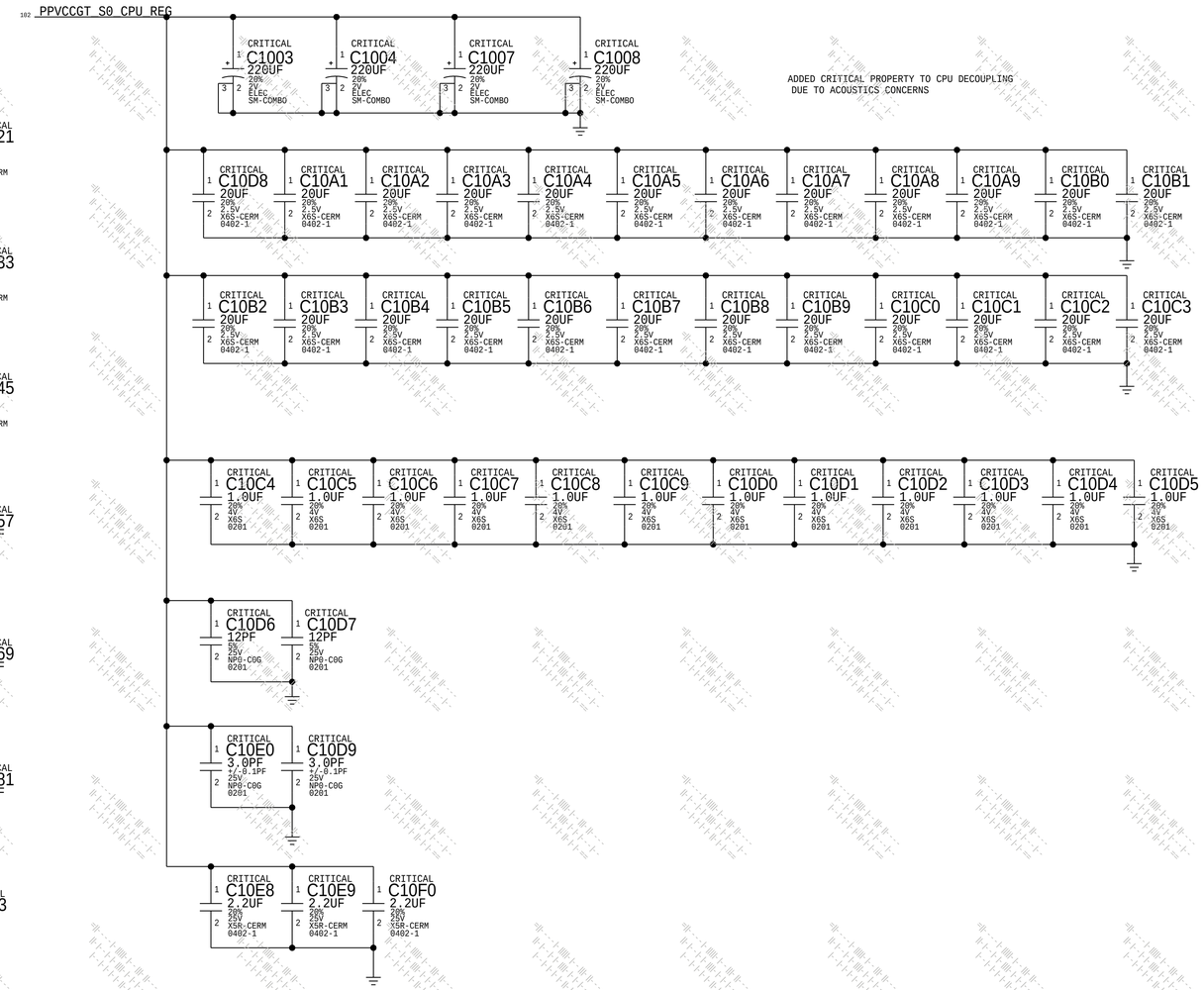
ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CPU GT DECOUPLING

INTEL RECOMMENDATION:2X 220uF Near CPU
3X 47uF 0805,7x 22uF 0603 @ board edge
10x 10uF 0402,12x 1uF 0201 @ back side

Apple Implementation: 4x 220uF
24x 20uF
12x 1uF
2X 12pF and 3pF

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



ADDED CRITICAL PROPERTY TO CPU DECOUPLING
DUE TO ACOUSTICS CONCERNS

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: CPU Decoupling 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 10 OF 142

SHEET: 10 OF 115

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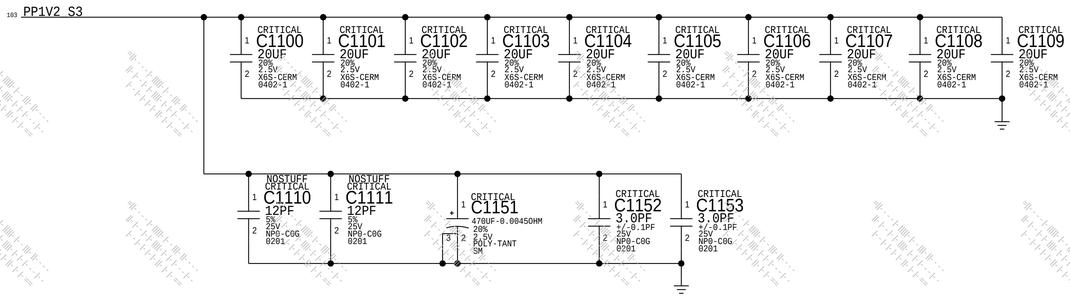
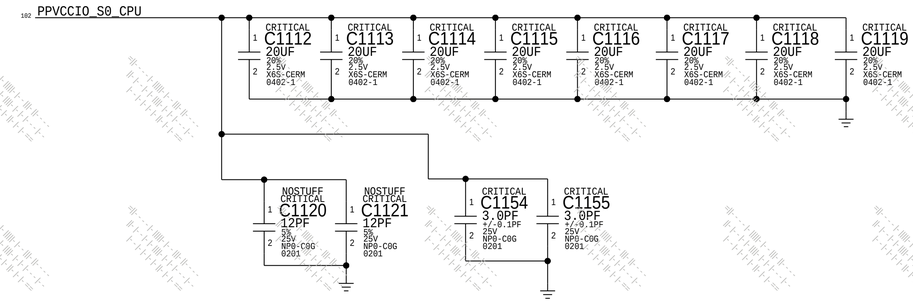
Memory (CPU VCCDDR) DECOUPLING

INTEL RECOMMENDATION:4X 22uF 0603,11x 10uF 0402 (back side)
Apple Implementation:10x 20uF
2x 12pF and 3pF (NO STUFF)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:2x 47UF 0805 near VR ouput
3x 10uF 0402,3x 0402 placeholder @ back side
Apple Implementation:8x 20uF
2x 12pF and 3pF (NO STUFF)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

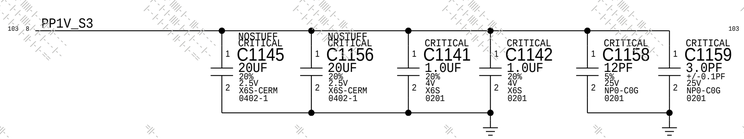


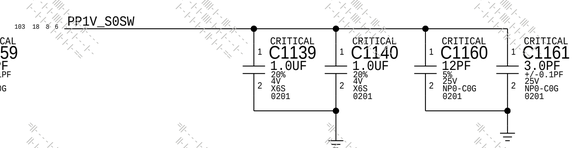
CPU VCCST / VCCSTG / VCCPLL / VCCPLL_OC DECOUPLING

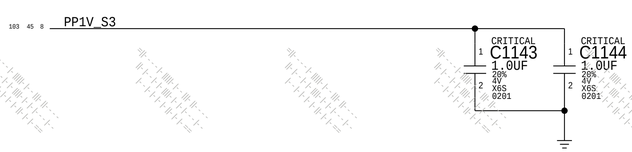
Intel Recommendation: VCCST: 1x 1uF 0201
VCCSTG: 1x 1uF 0201
VCCPLL: 1x 1uF 0201,1x 22uF/47uF 0805 placeholder
VCCPLL_OC: 2x 1uF 0201

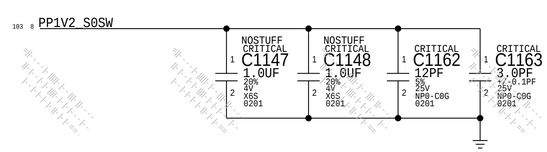
Apple Iimplementation: VCCST: 2x 1uF
VCCSTG: 2x 1uF
VCCPLL: 2x 20uF,2x 1uF
VCCPLL_OC: 2x 1uF

Layout Note: All these Must be Ground referenced.
VCCSTG board routing resistance from BGA to gate should less than 10mOhm.
Do not route VCCSTG closet adjcent layer over any power net other than GND.



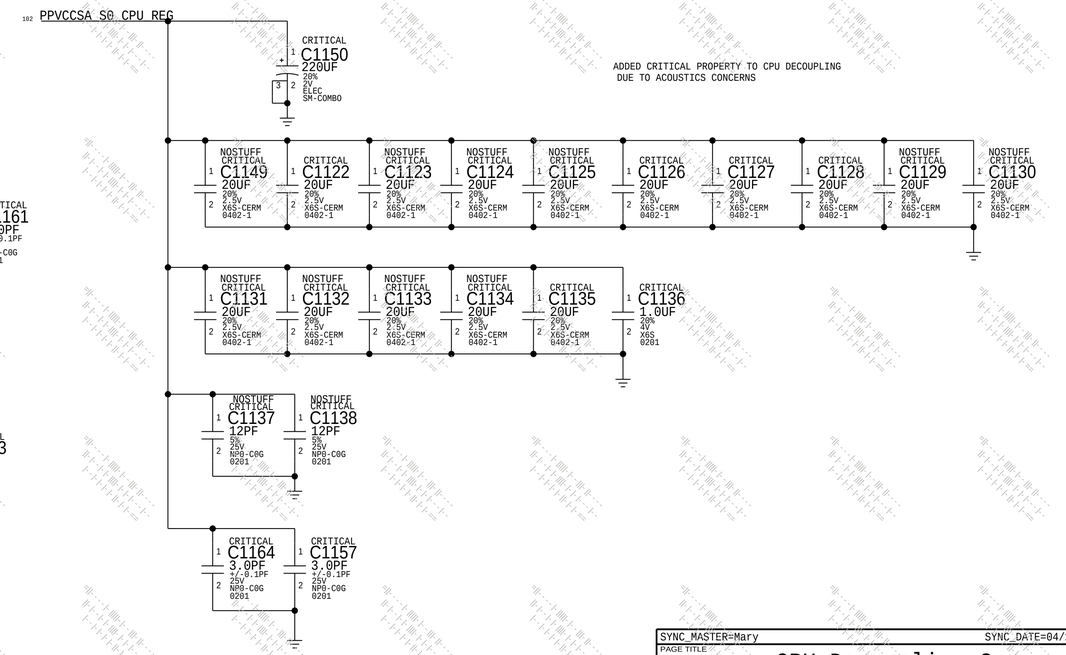






CPU VCCSA DECOUPLING

Intel Recommendation:2x 47uF 0805 near CPU
2x 47uF 0805,2x 22uF 0603 @ board edge
7x 10uF 0402,1x 1uF 0201 @ backside
Apple Implementation:1x 220uF
5x 20uF
1x 1uF
2x 12pF and 3pF (NO STUFF)



ADDED CRITICAL PROPERTY TO CPU DECOUPLING
DUE TO ACOUSTICS CONCERNS

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
CPU Decoupling 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 11 OF 142
SHEET 11 OF 115

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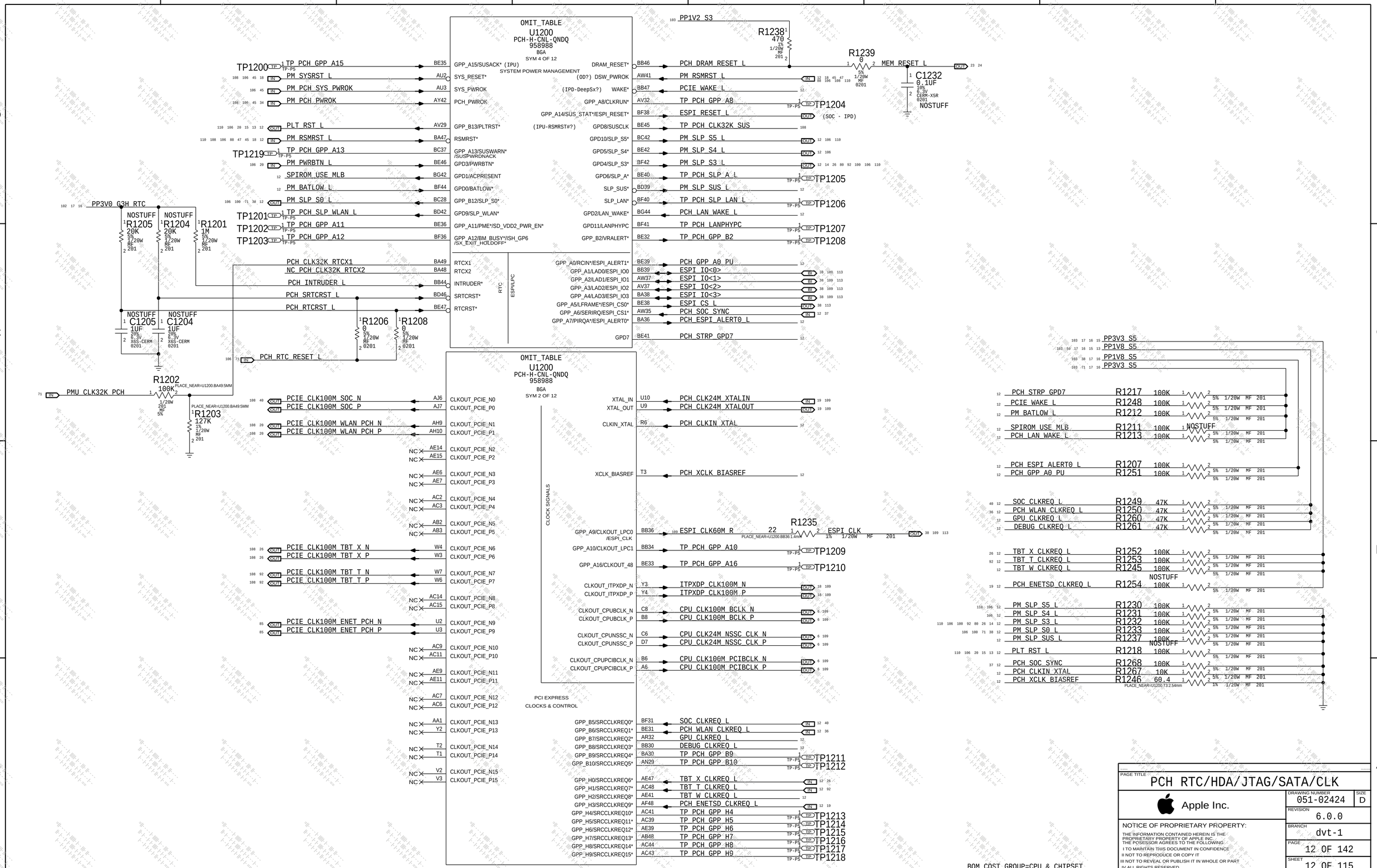
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 4 OF 12
SYSTEM POWER MANAGEMENT
GPP_A15/SUSACK* (IPU)
SYS_RESET*
SYS_PWROK
PCH_PWROK
GPP_B13/PLTRST*
RSMRST*
GPP_A13/SUSWARN* /SUSPWRDNACK
GPP3/PWRBTN*
GPD1/ACPRESENT
GPD0/BATLOW*
GPP_B12/SLP_S0*
GPD9/SLP_WLAN*
GPP_A11/PME*/SD_VDD2_PWR_EN*
GPP_A12/BM_BUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*
DRAM_RESET*
(OD?) DSW_PWROK
(IPD-DeepSx?) WAKE*
GPP_A8/CLKRUN*
GPP_A14/SUS_STAT*/ESPI_RESET*
(IPU-RSMRST#?) GPD8/SUSCLK
GPD10/SLP_S5*
GPD5/SLP_S4*
GPD4/SLP_S3*
GPD6/SLP_A*
SLP_SUS*
SLP_LAN*
GPD2/LAN_WAKE*
GPD11/LANPHYPC
GPP_B2/VRALERT*
RTCX1
RTCX2
INTRUDER*
SRTCRST*
RTCRST*
RTC
ESPI/LPC
GPP_A0/RCIN*/ESPI_ALERT1*
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME*/ESPI_CS0*
GPP_A6/SERIRQ/ESPI_CS1*
GPP_A7/PIRQA*/ESPI_ALERT0*
GPD7
TP1200 TP_PCH_GPP_A15
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PLT_RST_L
PM_RSMRST_L
TP1219 TP_PCH_GPP_A13
PM_PWRBTN_L
SPIROM_USE_MLB
PM_BATLOW_L
PM_SLP_S0_L
TP1201 TP_PCH_SLP_WLAN_L
TP1202 TP_PCH_GPP_A11
TP1203 TP_PCH_GPP_A12
PCH_CLK32K_RTCX1
NC_PCH_CLK32K_RTCX2
PCH_INTRUDER_L
PCH_SRTCRST_L
PCH_RTCRST_L
PCH_RTC_RESET_L
PP3V0_G3H_RTC
NOSTUFF R1205 20K 5% 1/20W MF 201
NOSTUFF R1204 20K 5% 1/20W MF 201
R1201 1M 5% 1/20W MF 201
NOSTUFF C1205 1UF 20% 6.3V X6S-CERM 0201
NOSTUFF C1204 1UF 20% 6.3V X6S-CERM 0201
R1206 0 5% 1/20W MF 0201
R1208 0 5% 1/20W MF 0201
R1202 100K 5% 1/20W MF 201
PMU_CLK32K_PCH
R1203 127K 1% 1/20W MF 201
PLACE_NEAR=U1200.BA49:5MM
PLACE_NEAR=U1200.BA49:5MM
PP1V2_S3
R1238 470 5% 1/20W MF 201
R1239 0 5% 1/20W MF 0201
MEM_RESET_L
C1232 0.1UF 10% 6.3V CERM-X5R 0201
NOSTUFF
PCH_DRAM_RESET_L
PM_RSMRST_L
PCIE_WAKE_L
TP_PCH_GPP_A8
TP1204
ESPI_RESET_L
(SOC - IPD)
TP_PCH_CLK32K_SUS
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PCH_SLP_A_L
TP1205
PM_SLP_SUS_L
TP_PCH_SLP_LAN_L
TP1206
PCH_LAN_WAKE_L
TP_PCH_LANPHYPC
TP1207
TP_PCH_GPP_B2
TP1208
PCH_GPP_A0_PU
ESPI_IO<0>
ESPI_IO<1>
ESPI_IO<2>
ESPI_IO<3>
ESPI_CS_L
PCH_SOC_SYNC
PCH_ESPI_ALERT0_L
PCH_STRP_GPD7
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 2 OF 12
CLOCK SIGNALS
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
PCIE_CLK100M_SOC_N
PCIE_CLK100M_SOC_P
PCIE_CLK100M_WLAN_PCH_N
PCIE_CLK100M_WLAN_PCH_P
PCIE_CLK100M_TBT_X_N
PCIE_CLK100M_TBT_X_P
PCIE_CLK100M_TBT_T_N
PCIE_CLK100M_TBT_T_P
PCIE_CLK100M_ENET_PCH_N
PCIE_CLK100M_ENET_PCH_P
XTAL_IN
XTAL_OUT
CLKIN_XTAL
PCH_CLK24M_XTALIN
PCH_CLK24M_XTALOUT
PCH_CLKIN_XTAL
XCLK_BIASREF
PCH_XCLK_BIASREF
GPP_A9/CLKOUT_LPC0 /ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A16/CLKOUT_48
ESPI_CLK60M_R
R1235 22 1% 1/20W MF 201
PLACE_NEAR=U1200.BB36:1.4mm
ESPI_CLK
TP_PCH_GPP_A10
TP1209
TP_PCH_GPP_A16
TP1210
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUBCLK_P
CPU_CLK100M_BCLK_N
CPU_CLK100M_BCLK_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUNSSC_P
CPU_CLK24M_NSSC_CLK_N
CPU_CLK24M_NSSC_CLK_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
CPU_CLK100M_PCIBCLK_N
CPU_CLK100M_PCIBCLK_P
PCI EXPRESS
CLOCKS & CONTROL
GPP_B5/SRCCLKREQ0*
GPP_B6/SRCCLKREQ1*
GPP_B7/SRCCLKREQ2*
GPP_B8/SRCCLKREQ3*
GPP_B9/SRCCLKREQ4*
GPP_B10/SRCCLKREQ5*
GPP_H0/SRCCLKREQ6*
GPP_H1/SRCCLKREQ7*
GPP_H2/SRCCLKREQ8*
GPP_H3/SRCCLKREQ9*
GPP_H4/SRCCLKREQ10*
GPP_H5/SRCCLKREQ11*
GPP_H6/SRCCLKREQ12*
GPP_H7/SRCCLKREQ13*
GPP_H8/SRCCLKREQ14*
GPP_H9/SRCCLKREQ15*
SOC_CLKREQ_L
PCH_WLAN_CLKREQ_L
GPU_CLKREQ_L
DEBUG_CLKREQ_L
TP_PCH_GPP_B9
TP1211
TP_PCH_GPP_B10
TP1212
TBT_X_CLKREQ_L
TBT_T_CLKREQ_L
TBT_W_CLKREQ_L
PCH_ENETSD_CLKREQ_L
TP_PCH_GPP_H4
TP1213
TP_PCH_GPP_H5
TP1214
TP_PCH_GPP_H6
TP1215
TP_PCH_GPP_H7
TP1216
TP_PCH_GPP_H8
TP1217
TP_PCH_GPP_H9
TP1218
PP3V3_S5
PP1V8_S5
PP1V8_S5
PP3V3_S5
PCH_STRP_GPD7 R1217 100K 5% 1/20W MF 201
PCIE_WAKE_L R1248 100K 5% 1/20W MF 201
PM_BATLOW_L R1212 100K 5% 1/20W MF 201
SPIROM_USE_MLB R1211 100K 5% 1/20W MF 201 NOSTUFF
PCH_LAN_WAKE_L R1213 100K 5% 1/20W MF 201
PCH_ESPI_ALERT0_L R1207 100K 5% 1/20W MF 201
PCH_GPP_A0_PU R1251 100K 5% 1/20W MF 201
SOC_CLKREQ_L R1249 47K 5% 1/20W MF 201
PCH_WLAN_CLKREQ_L R1250 47K 5% 1/20W MF 201
GPU_CLKREQ_L R1260 47K 5% 1/20W MF 201
DEBUG_CLKREQ_L R1261 47K 5% 1/20W MF 201
TBT_X_CLKREQ_L R1252 100K 5% 1/20W MF 201
TBT_T_CLKREQ_L R1253 100K 5% 1/20W MF 201
TBT_W_CLKREQ_L R1245 100K 5% 1/20W MF 201
NOSTUFF
PCH_ENETSD_CLKREQ_L R1254 100K 5% 1/20W MF 201
PM_SLP_S5_L R1230 100K 5% 1/20W MF 201
PM_SLP_S4_L R1231 100K 5% 1/20W MF 201
PM_SLP_S3_L R1232 100K 5% 1/20W MF 201
PM_SLP_S0_L R1233 100K 5% 1/20W MF 201
PM_SLP_SUS_L R1237 100K 5% 1/20W MF 201
NOSTUFF
PLT_RST_L R1218 100K 5% 1/20W MF 201
PCH_SOC_SYNC R1268 100K 5% 1/20W MF 201
PCH_CLKIN_XTAL R1267 10K 5% 1/20W MF 201
PCH_XCLK_BIASREF R1246 60.4 1% 1/20W MF 201
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BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 12 OF 142
SHEET 12 OF 115
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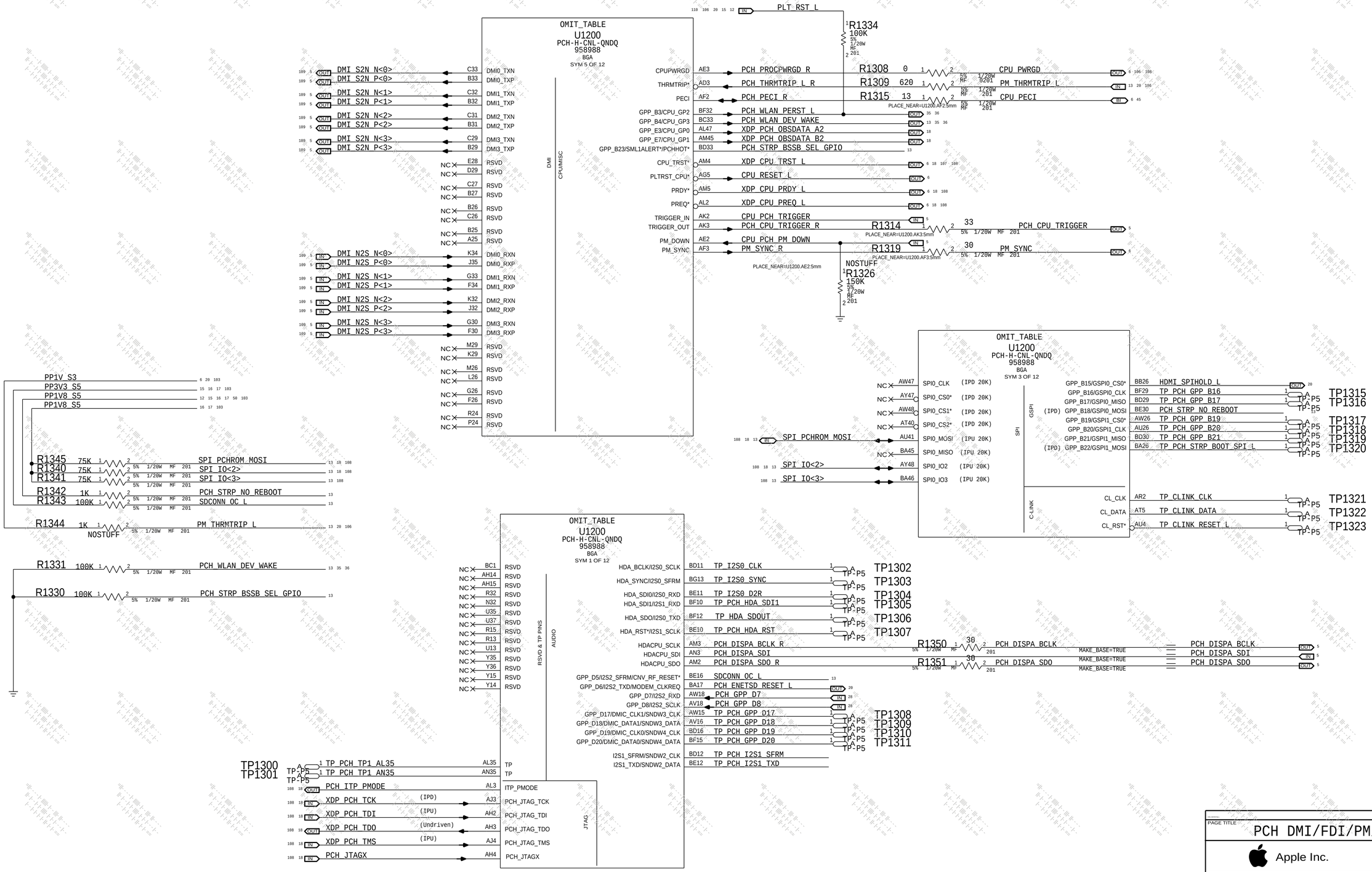

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
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SHEET 13 OF 115

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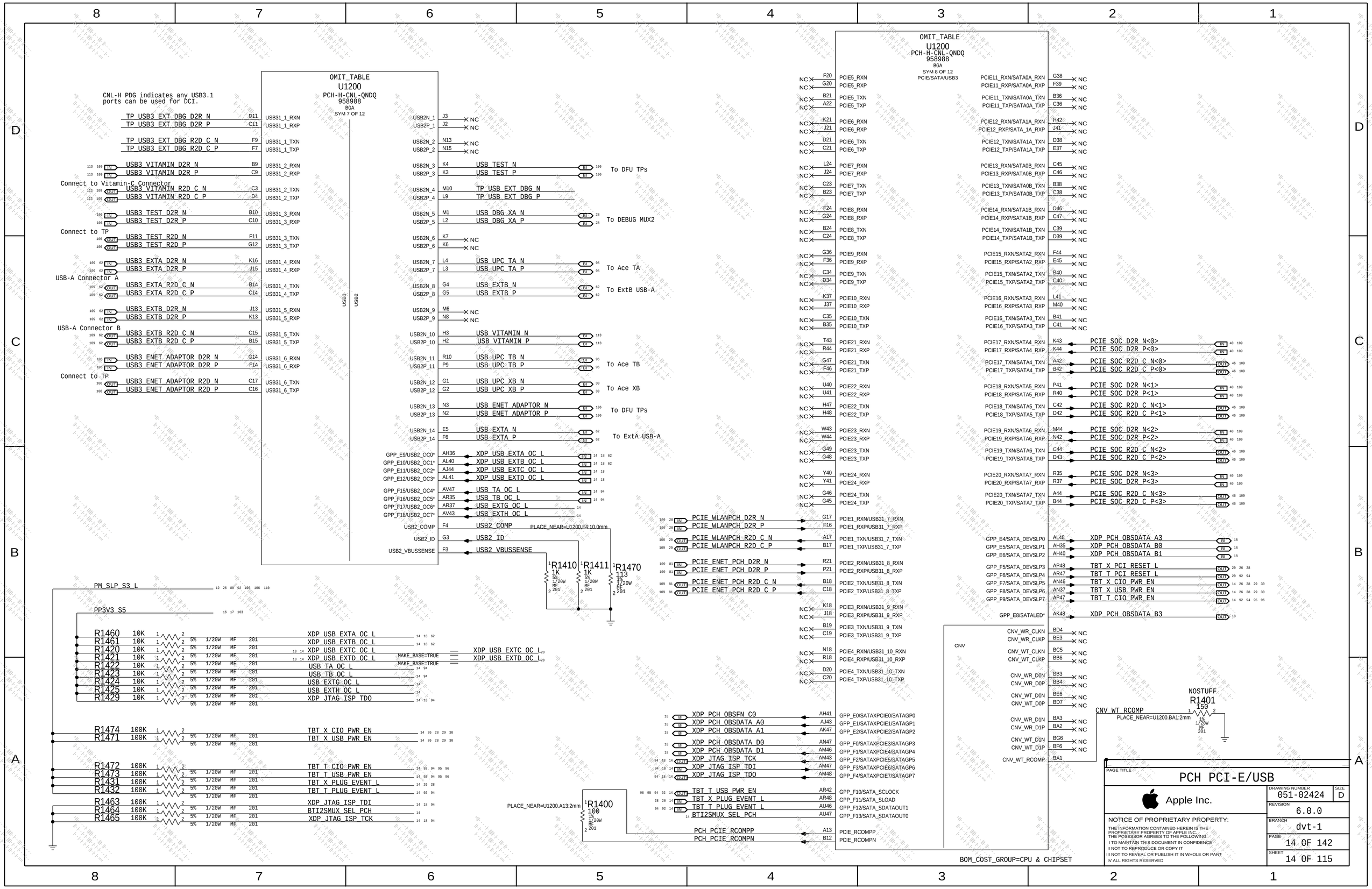
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 7 OF 12
CNL-H PDG indicates any USB3.1 ports can be used for DCI.
TP_USB3_EXT_DBG_D2R_N
TP_USB3_EXT_DBG_D2R_P
TP_USB3_EXT_DBG_R2D_C_N
TP_USB3_EXT_DBG_R2D_C_P
USB3_VITAMIN_D2R_N
USB3_VITAMIN_D2R_P
Connect to Vitamin-C Connector
USB3_VITAMIN_R2D_C_N
USB3_VITAMIN_R2D_C_P
USB3_TEST_D2R_N
USB3_TEST_D2R_P
Connect to TP
USB3_TEST_R2D_N
USB3_TEST_R2D_P
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB-A Connector A
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
USB-A Connector B
USB3_EXTB_R2D_C_N
USB3_EXTB_R2D_C_P
USB3_ENET_ADAPTOR_D2R_N
USB3_ENET_ADAPTOR_D2R_P
Connect to TP
USB3_ENET_ADAPTOR_R2D_N
USB3_ENET_ADAPTOR_R2D_P
USB3_TEST_N
USB3_TEST_P
To DFU TPs
TP_USB_EXT_DBG_N
TP_USB_EXT_DBG_P
USB_DBG_XA_N
USB_DBG_XA_P
To DEBUG MUX2
USB_UPC_TA_N
USB_UPC_TA_P
To Ace TA
USB_EXTB_N
USB_EXTB_P
To ExtB USB-A
USB_VITAMIN_N
USB_VITAMIN_P
USB_UPC_TB_N
USB_UPC_TB_P
To Ace TB
USB_UPC_XB_N
USB_UPC_XB_P
To Ace XB
USB_ENET_ADAPTOR_N
USB_ENET_ADAPTOR_P
To DFU TPs
USB_EXTA_N
USB_EXTA_P
To ExtA USB-A
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
USB_TA_OC_L
USB_TB_OC_L
USB_EXTG_OC_L
USB_EXTH_OC_L
USB2_COMP
USB2_ID
USB2_VBUSSENSE
PLACE_NEAR=U1200.F4:10.0mm
R1410 1K
R1411 1K
R1470 113
PM_SLP_S3_L
PP3V3_S5
R1460 10K XDP_USB_EXTA_OC_L
R1461 10K XDP_USB_EXTB_OC_L
R1420 10K XDP_USB_EXTC_OC_L
R1421 10K XDP_USB_EXTD_OC_L
R1422 10K USB_TA_OC_L
R1423 10K USB_TB_OC_L
R1424 10K USB_EXTG_OC_L
R1425 10K USB_EXTH_OC_L
R1429 10K XDP_JTAG_ISP_TDO
MAKE_BASE=TRUE
R1474 100K TBT_X_CIO_PWR_EN
R1471 100K TBT_X_USB_PWR_EN
R1472 100K TBT_T_CIO_PWR_EN
R1473 100K TBT_T_USB_PWR_EN
R1431 100K TBT_X_PLUG_EVENT_L
R1432 100K TBT_T_PLUG_EVENT_L
R1463 100K XDP_JTAG_ISP_TDI
R1464 100K BTI2SMUX_SEL_PCH
R1465 100K XDP_JTAG_ISP_TCK
PLACE_NEAR=U1200.A13:2mm
R1400 100
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 8 OF 12
PCIE/SATA/USB3
PCIE_WLANPCH_D2R_N
PCIE_WLANPCH_D2R_P
PCIE_WLANPCH_R2D_C_N
PCIE_WLANPCH_R2D_C_P
PCIE_ENET_PCH_D2R_N
PCIE_ENET_PCH_D2R_P
PCIE_ENET_PCH_R2D_C_N
PCIE_ENET_PCH_R2D_C_P
XDP_PCH_OBSFN_C0
XDP_PCH_OBSDATA_A0
XDP_PCH_OBSDATA_A1
XDP_PCH_OBSDATA_D0
XDP_PCH_OBSDATA_D1
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI
XDP_JTAG_ISP_TDO
TBT_T_USB_PWR_EN
TBT_X_PLUG_EVENT_L
TBT_T_PLUG_EVENT_L
BTI2SMUX_SEL_PCH
PCH_PCIE_RCOMPP
PCH_PCIE_RCOMPN
PCIE_SOC_D2R_N<0>
PCIE_SOC_D2R_P<0>
PCIE_SOC_R2D_C_N<0>
PCIE_SOC_R2D_C_P<0>
PCIE_SOC_D2R_N<1>
PCIE_SOC_D2R_P<1>
PCIE_SOC_R2D_C_N<1>
PCIE_SOC_R2D_C_P<1>
PCIE_SOC_D2R_N<2>
PCIE_SOC_D2R_P<2>
PCIE_SOC_R2D_C_N<2>
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PCIE_SOC_D2R_N<3>
PCIE_SOC_D2R_P<3>
PCIE_SOC_R2D_C_N<3>
PCIE_SOC_R2D_C_P<3>
XDP_PCH_OBSDATA_A3
XDP_PCH_OBSDATA_B0
XDP_PCH_OBSDATA_B1
TBT_X_PCI_RESET_L
TBT_T_PCI_RESET_L
TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN
TBT_T_CIO_PWR_EN
XDP_PCH_OBSDATA_B3
CNV
CNV_WT_RCOMP
PLACE_NEAR=U1200.BA1:2mm
NOSTUFF
R1401 150
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 14 OF 142
SHEET 14 OF 115
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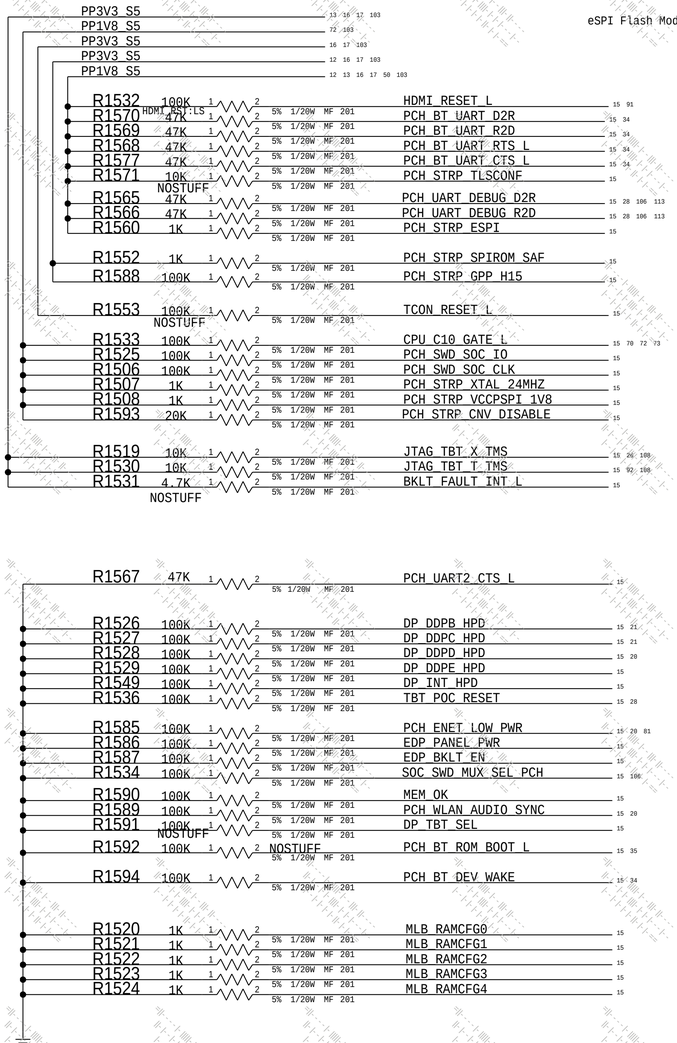
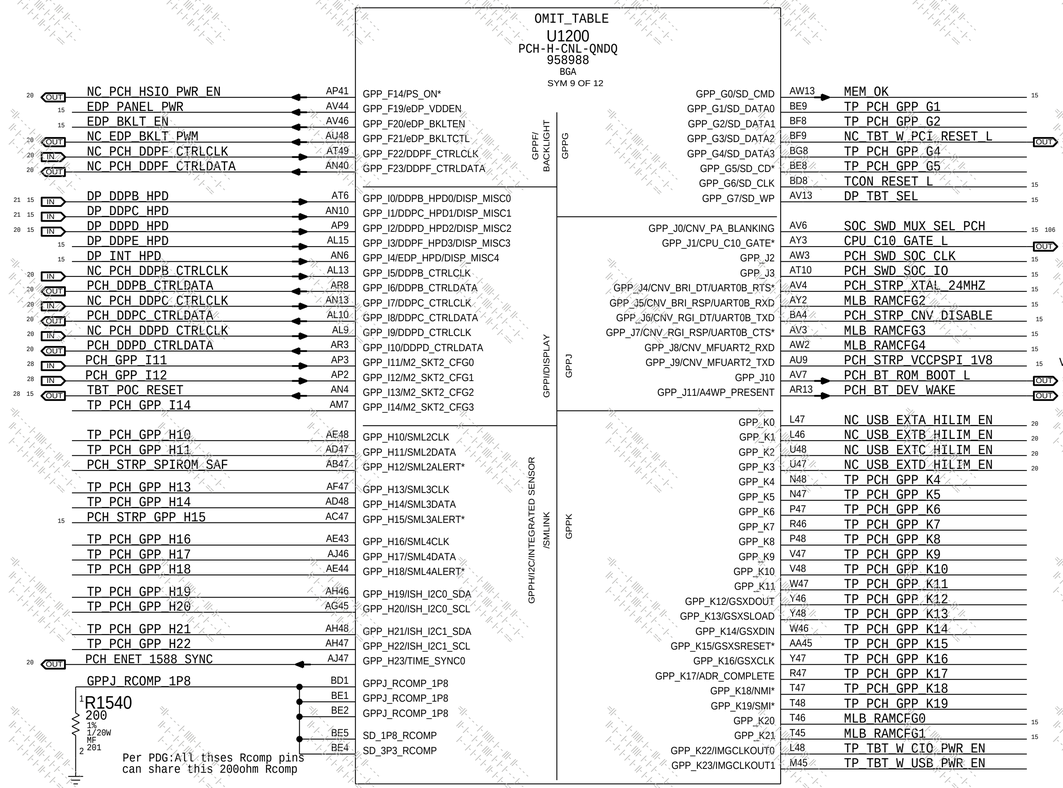
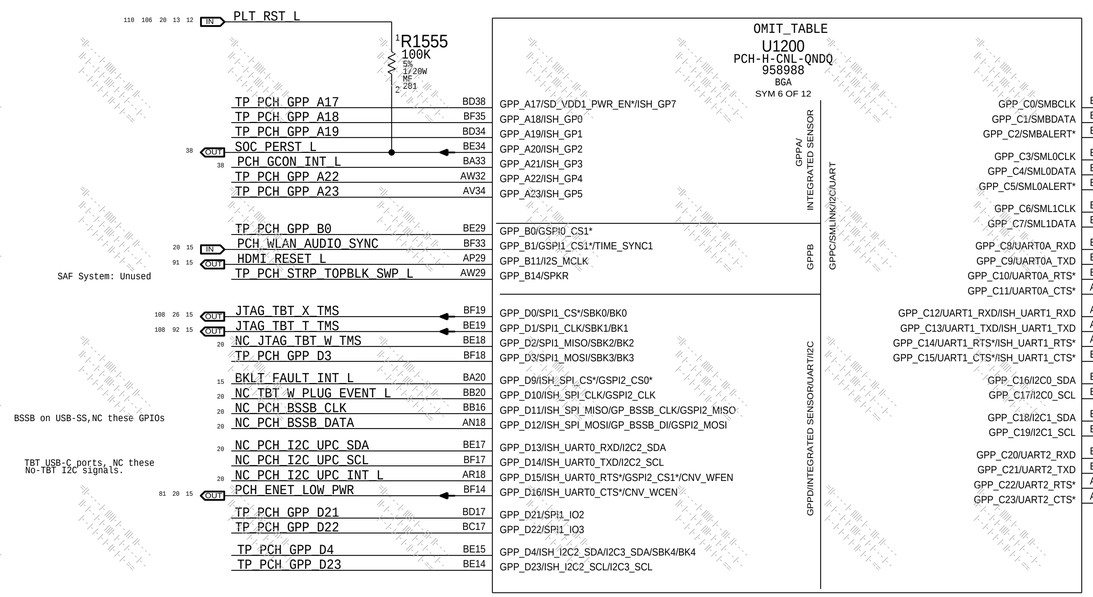


eSPI Flash Mode:0=MAF(not supported),1=SAF



If useing 38.4Mhz->PCH_STRP_XTAL38P4MHZ_L
DIMM config, no need to check RAMCFG

VCCSPI: 0=3.3V,1=1.8V



SAF System: Unused

BSSB on USB-SS,NC these GPIOs

TBT_USB-C ports, NC these NO-TBT I2C signals.

SMBus connects to DIMMs

Bus NOT used, only PUs

Strap:0=LPC,1=eSPI

Bus NOT used, only PUs

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
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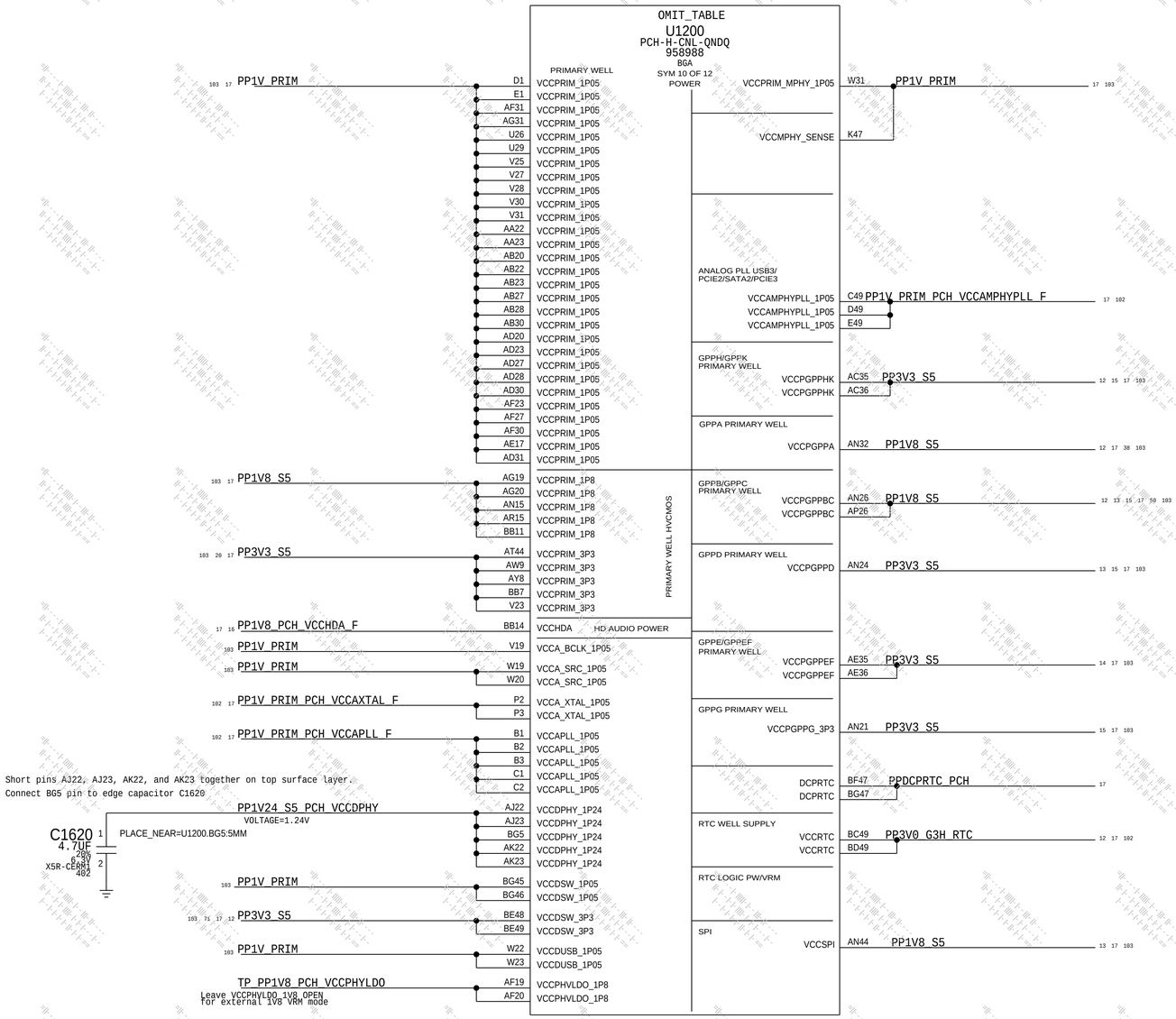
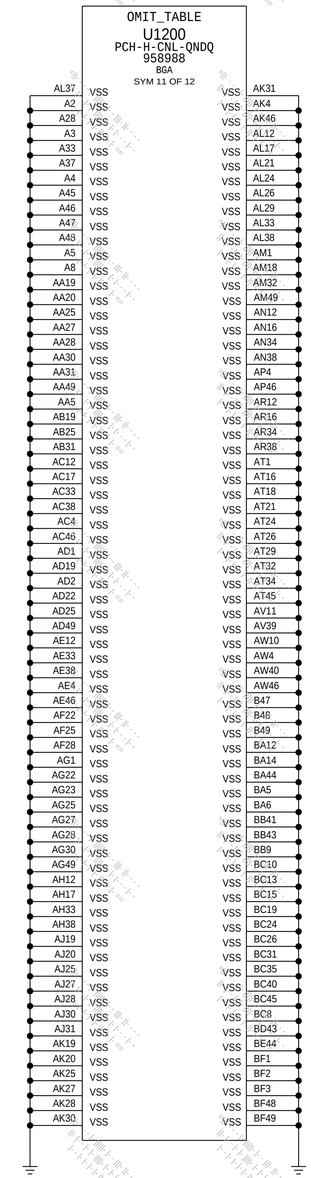
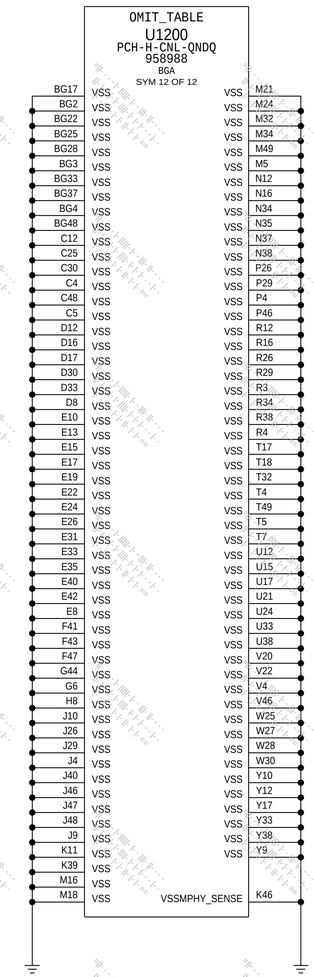
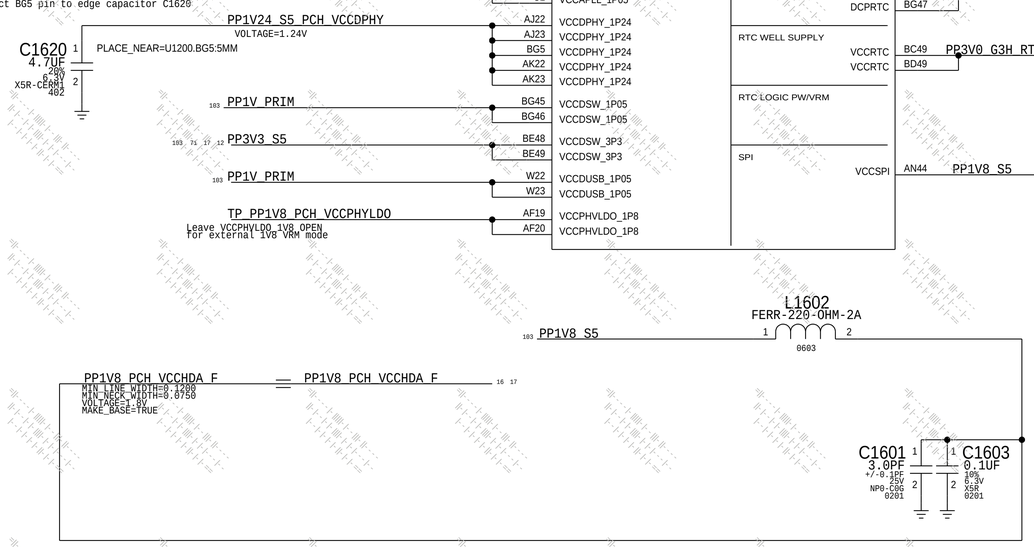






Short pins AJ22, AJ23, AK22, and AK23 together on top surface layer.
Connect BG5 pin to edge capacitor C1620



Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH Power

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DRAWING NUMBER	051-02424
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1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED

PLACE_NEAR=U1200.AF31:3MM
PP1V_PRIM
C1743 1UF 10% 6.3V CERM 402
C1750 12PF 5% 50V NP0-C0G 0201
C1730 0.1UF 10% 10V X5R-CERM 0201
C1731 0.1UF 10% 10V X5R-CERM 0201
C1732 0.1UF 10% 10V X5R-CERM 0201
C76 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U1200.U26:5MM
C1700 22UF 20% 6.3V X5R-CERM-1 603
PLACE_NEAR=U1200.V27:3MM
C1701 1UF 10% 6.3V CERM 402

PLACE_NEAR=U1200.AA23:1.4MM
PP1V_PRIM
C1751 12PF 5% 50V NP0-C0G 0201
C1736 47UF 20% 6.3V POLY-TANT 0805
C1737 1UF 20% 6.3V X6S-CERM 0201
C1734 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U1200.AD31:2.1MM
C1735 0.1UF 10% 10V X5R-CERM 0201
C1738 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U1200.AF31:1MM
C1702 1UF 20% 6.3V X6S-CERM 0201

PLACE_NEAR=U1200.V25:1MM
PP1V_PRIM
PLACE_NEAR=U1200.AF23:1MM
C1739 0.1UF 10% 10V X5R-CERM 0201
C1703 1UF 20% 6.3V X6S-CERM 0201

PLACE_NEAR=U1200.BF47:3MM
PPDCPRTC_PCH
VOLTAGE=2.0V
C1709 0.1UF 10% 10V X5R-CERM 0201

PLACE_NEAR=U1200.BC49:1MM
PP3V0_G3H_RTC
PLACE_NEAR=U1200.BC49:1MM
NOSTUFF C1745 1UF 20% 6.3V X6S-CERM 0201
NOSTUFF C1715 0.1UF 10% 10V X5R-CERM 0201

Change 1V8_S0_PCH_VCCHDA to 1V8_PCH_VCCHDA_F
Because PCH is using 1V8_PRIM instead of 1V8_S0.
PP1V8_PCH_VCCHDA_F
PLACE_NEAR=U1200.BB14:1.2MM
PLACE_NEAR=U1200.BB14:1.2MM
C1749 0.1UF 10% 10V X5R-CERM 0201
C1748 22UF 20% 6.3V X5R-CERM-1 603
C1717 1UF 20% 6.3V X6S-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.BB7:3MM
C1744 47UF 20% 6.3V POLY-TANT 0805
C1752 12PF 5% 50V NP0-C0G 0201
C1719 1UF 20% 6.3V X6S-CERM 0201
C1720 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U1200.AY8:3MM

PP3V3_S5
C1753 12PF 5% 50V NP0-C0G 0201
C1723 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U1200.BE49:1MM
C1724 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U1200.BE48:1MM

PP1V8_S5
PLACE_NEAR=U1200.AN44:1MM
C1757 0.1UF 10% 10V X5R-CERM 0201

PP1V8_S5
PLACE_NEAR=U1200.AG19:3MM
C1762 1UF 20% 6.3V X6S-CERM 0201

PP1V_PRIM
PLACE_NEAR=U1200.AB30:1MM
C1708 1UF 20% 6.3V X6S-CERM 0201

PP1V8_S5
PLACE_NEAR=U1200.AN26:1MM
C1710 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AE35:1MM
C1713 0.1UF 10% 10V X5R-CERM 0201

PP1V8_S5
PLACE_NEAR=U1200.AN32:1MM
C1746 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AC35:1MM
C1733 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AN21:3MM
C1747 22UF 20% 6.3V X5R-CERM-1 603
PLACE_NEAR=U1200.AN21:3MM
C1714 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.AN24:3MM
C1716 0.1UF 10% 10V X5R-CERM 0201

PP3V3_S5
PLACE_NEAR=U1200.BE49:3MM
C1718 1UF 20% 6.3V X6S-CERM 0201

PP3V0_G3H_RTC
PLACE_NEAR=U1200.BD49:3MM
C1721 1UF 20% 6.3V X6S-CERM 0201
PLACE_NEAR=U1200.BD49:3MM
C1722 0.1UF 10% 10V X5R-CERM 0201

RAIL SIDE
PCH SIDE

PP1V_PRIM
C1754 12PF 5% 50V NP0-C0G 0201
L1700 2.2UH-20%-0.19A-0.2210HM 0603
PLACE_NEAR=U1200.C49:5MM
PLACE_NEAR=U1200.C49:3MM
C1704 22UF 20% 6.3V X5R-CERM 0603-1
PLACE_NEAR=U1200.D49:3MM
C1740 0.1UF 10% 10V X5R-CERM 0201
PLACE_NEAR=U1200.E49:3MM
C1705 1UF 20% 6.3V X6S-CERM 0201
PP1V_PRIM_PCH_VCCAMPHYPLL_F

PP1V_PRIM
C1755 12PF 5% 50V NP0-C0G 0201
L1701 2.2UH-20%-0.19A-0.2210HM 0603
PLACE_NEAR=U1200.P2:1MM
PLACE_NEAR=U1200.P2:1MM
C1706 22UF 20% 6.3V X5R-CERM 0603-1
PLACE_NEAR=U1200.P2:1MM
C1741 0.1UF 10% 10V X5R-CERM 0201
C1707 1UF 20% 6.3V X6S-CERM 0201
PP1V_PRIM_PCH_VCCAXTAL_F
PLACE_NEAR=U1200.P3:1MM

PLACE_NEAR=U1200.B3:5MM
PLACE_NEAR=U1200.B1:5MM
PLACE_NEAR=U1200.C2:5MM
PP1V_PRIM
C1756 3.0PF +/-0.1PF 50V NP0-C0G 0201
L1702 2.2UH-20%-0.19A-0.2210HM 0603
PLACE_NEAR=U1200.B1:5MM
C1711 22UF 20% 6.3V X5R-CERM 0603-1
C1742 0.1UF 10% 10V X5R-CERM 0201
C1712 1UF 20% 6.3V X6S-CERM 0201
PP1V_PRIM_PCH_VCCAPLL_F

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: PCH Decoupling

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 17 OF 142
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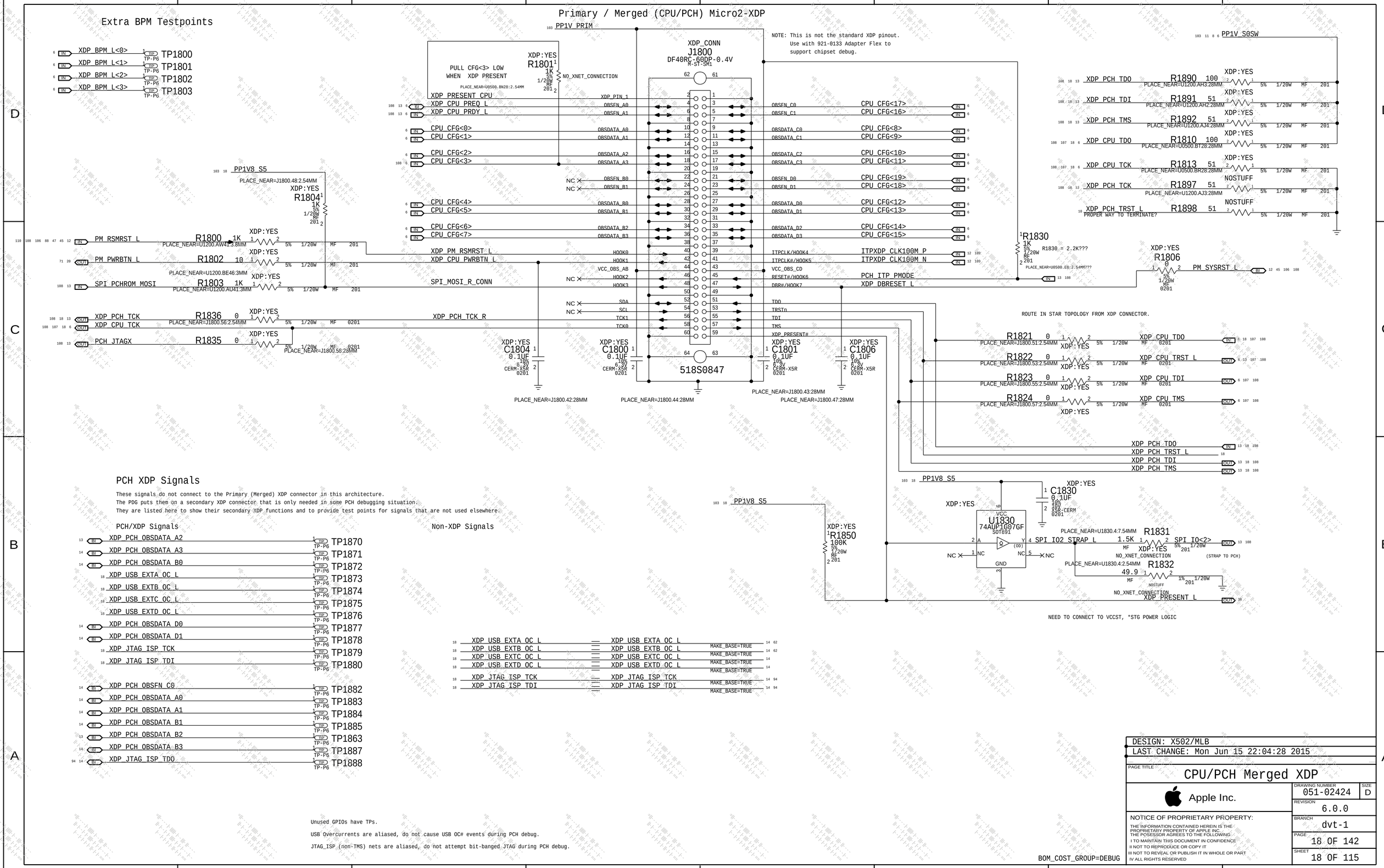
Extra BPM Testpoints
XDP_BPM_L<0> TP1800
XDP_BPM_L<1> TP1801
XDP_BPM_L<2> TP1802
XDP_BPM_L<3> TP1803
Primary / Merged (CPU/PCH) Micro2-XDP
PP1V_PRIM
PULL CFG<3> LOW WHEN XDP PRESENT
R1801 1K NO_XNET_CONNECTION
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847
NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.
PP1V_S0SW
XDP_PCH_TDO R1890 100
XDP_PCH_TDI R1891 51
XDP_PCH_TMS R1892 51
XDP_CPU_TDO R1810 100
XDP_CPU_TCK R1813 51
XDP_PCH_TCK R1897 51
XDP_PCH_TRST_L R1898 51
PROPER WAY TO TERMINATE?
PP1V8_S5
R1804 1K
PM_RSMRST_L R1800 1K
PM_PWRBTN_L R1802 10
SPI_PCHROM_MOSI R1803 1K
XDP_PCH_TCK R1836 0
XDP_CPU_TCK
PCH_JTAGX R1835 0
R1830 1K
R1830 = 2.2K???
R1806 0
PM_SYSRST_L
ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.
R1821 0 XDP_CPU_TDO
R1822 0 XDP_CPU_TRST_L
R1823 0 XDP_CPU_TDI
R1824 0 XDP_CPU_TMS
XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS
C1804 0.1UF
C1800 0.1UF
C1801 0.1UF
C1806 0.1UF
PCH XDP Signals
These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.
PCH/XDP Signals
XDP_PCH_OBSDATA_A2 TP1870
XDP_PCH_OBSDATA_A3 TP1871
XDP_PCH_OBSDATA_B0 TP1872
XDP_USB_EXTA_OC_L TP1873
XDP_USB_EXTB_OC_L TP1874
XDP_USB_EXTC_OC_L TP1875
XDP_USB_EXTD_OC_L TP1876
XDP_PCH_OBSDATA_D0 TP1877
XDP_PCH_OBSDATA_D1 TP1878
XDP_JTAG_ISP_TCK TP1879
XDP_JTAG_ISP_TDI TP1880
XDP_PCH_OBSFN_C0 TP1882
XDP_PCH_OBSDATA_A0 TP1883
XDP_PCH_OBSDATA_A1 TP1884
XDP_PCH_OBSDATA_B1 TP1885
XDP_PCH_OBSDATA_B2 TP1863
XDP_PCH_OBSDATA_B3 TP1887
XDP_JTAG_ISP_TDO TP1888
Non-XDP Signals
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI
MAKE_BASE=TRUE
PP1V8_S5
R1850 100K
U1830 74AUP1G07GF SOT891
C1830 0.1UF
R1831 1.5K SPI_IO2_STRAP_L
SPI_IO<2> (STRAP TO PCH)
R1832 49.9
XDP_PRESENT_L
NEED TO CONNECT TO VCCST, *STG POWER LOGIC
Unused GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
BOM_COST_GROUP=DEBUG
DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015
PAGE TITLE
CPU/PCH Merged XDP
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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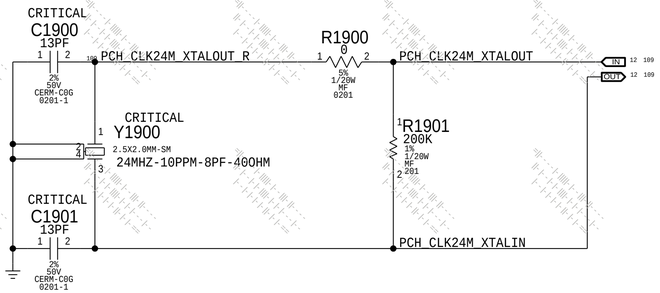
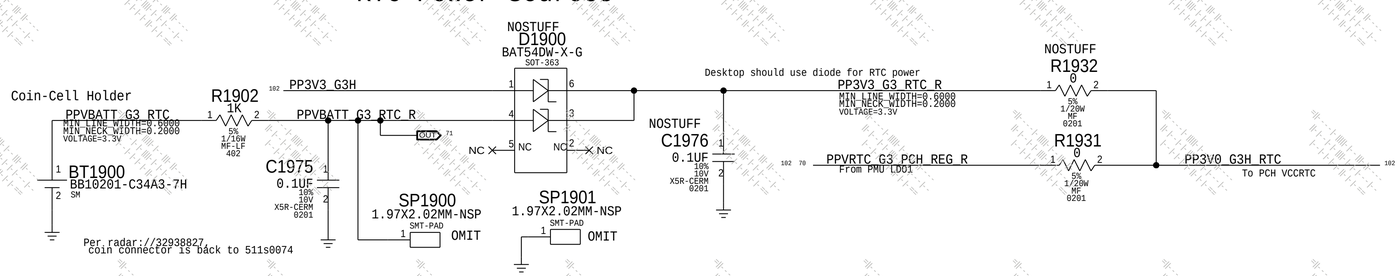
PCH 24MHz Crystal



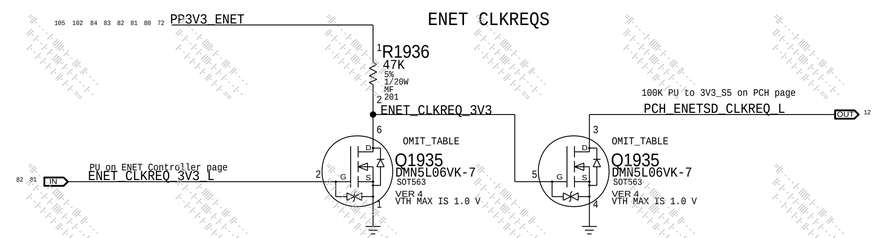
CL (load capacitance) = 8pF
Cs (trace capacitance) = 1pF (assumption)
Ci (package capacitance) = 0.5pF (assumption)
Ce = 2 * (CL - Cs - Ci) = 2 * (8 - 1 -0.5) = 13pF

PDG recommends 18pF,check in charz.

RTC Power Sources



Per radar://32938827
Coin connector is back to 511s0074



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	Chipset Support 1
	Apple Inc.
DRAWING NUMBER	051-02424
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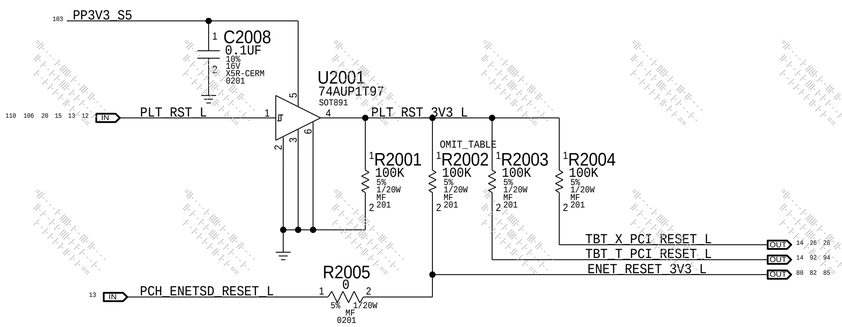
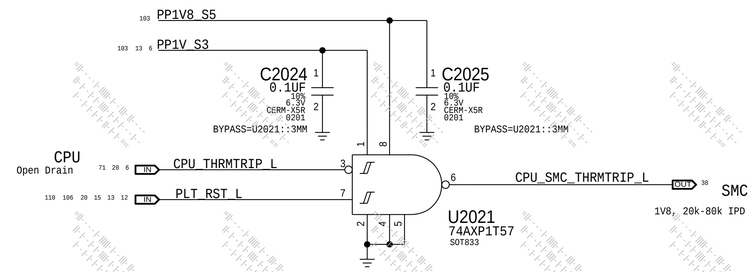
Platform Reset Level Shifter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, 100K	R2002		ENET:10G
117S0006	1	RES, 1K	R2002		ENET:1G



PMU response will be overridden by SMC, unless SMC and/or PCH is hung.

Misc Alias

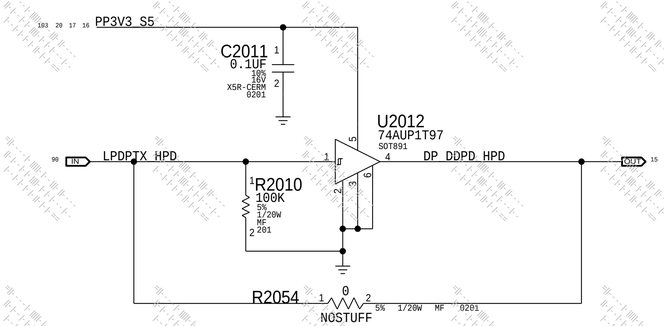
PM_PWRBTN_L		PM_PWRBTN_L MAKE_BASE=TRUE
PCIE_WLANPCH_D2R_N	MAKE_BASE=TRUE	PCIE_WLANPCH_D2R_N
PCIE_WLANPCH_D2R_P	MAKE_BASE=TRUE	PCIE_WLANPCH_D2R_P
PCIE_WLANPCH_R2D_C_N	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_N
PCIE_WLANPCH_R2D_C_P	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_P
PCIE_WLANPCH_R2D_C_N	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_N
PCIE_WLANPCH_R2D_C_P	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_P
PCIE_CLK100M_WLAN_PCH_N	MAKE_BASE=TRUE	PCIE_CLK100M_WLAN_PCH_N
PCIE_CLK100M_WLAN_PCH_P	MAKE_BASE=TRUE	PCIE_CLK100M_WLAN_PCH_P

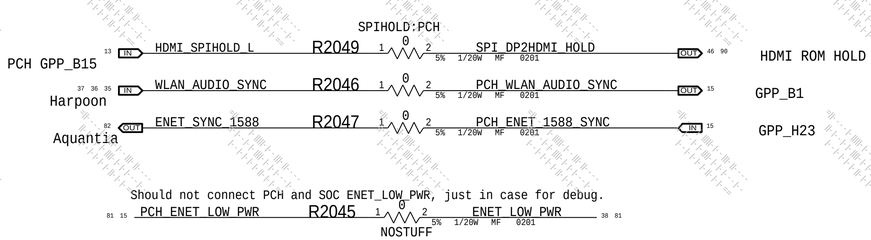
PCH NC Pins

NC_PCH_HSIO_PWR_EN		NC_PCH_HSIO_PWR_EN
NC_EDP_BKLT_PWM		NC_EDP_BKLT_PWM MAKE_BASE=TRUE
NC_PCH_DDPF_CTRLCLK		NC_PCH_DDPF_CTRLCLK MAKE_BASE=TRUE
NC_PCH_DDPF_CTRLDATA		NC_PCH_DDPF_CTRLDATA MAKE_BASE=TRUE
NC_PCH_DDPB_CTRLCLK		NC_PCH_DDPB_CTRLCLK MAKE_BASE=TRUE
NC_PCH_DDPC_CTRLCLK		NC_PCH_DDPC_CTRLCLK MAKE_BASE=TRUE
NC_PCH_DDPD_CTRLCLK		NC_PCH_DDPD_CTRLCLK MAKE_BASE=TRUE
NC_TBT_W_PCI_RESET_L		NC_TBT_W_PCI_RESET_L MAKE_BASE=TRUE
NC_USB_EXTA_HILIM_EN		NC_USB_EXTA_HILIM_EN MAKE_BASE=TRUE
NC_USB_EXTB_HILIM_EN		NC_USB_EXTB_HILIM_EN MAKE_BASE=TRUE
NC_USB_EXTC_HILIM_EN		NC_USB_EXTC_HILIM_EN MAKE_BASE=TRUE
NC_USB_EXTD_HILIM_EN		NC_USB_EXTD_HILIM_EN MAKE_BASE=TRUE
NC_JTAG_TBT_W_TMS		NC_JTAG_TBT_W_TMS MAKE_BASE=TRUE
NC_TBT_W_PLUG_EVENT_L		NC_TBT_W_PLUG_EVENT_L MAKE_BASE=TRUE
NC_PCH_BSSB_CLK		NC_PCH_BSSB_CLK MAKE_BASE=TRUE
NC_PCH_BSSB_DATA		NC_PCH_BSSB_DATA MAKE_BASE=TRUE
NC_PCH_I2C_UPC_SDA		NC_PCH_I2C_UPC_SDA MAKE_BASE=TRUE
NC_PCH_I2C_UPC_SCL		NC_PCH_I2C_UPC_SCL MAKE_BASE=TRUE
NC_PCH_I2C_UPC_INT_L		NC_PCH_I2C_UPC_INT_L MAKE_BASE=TRUE

PCH THRMTRIP connection

HDMI HPD





Display Port DDPB, DDPC,DDPD

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	Chipset Support 2
Apple Inc.	
DRAWING NUMBER	051-02424
SIZE	D
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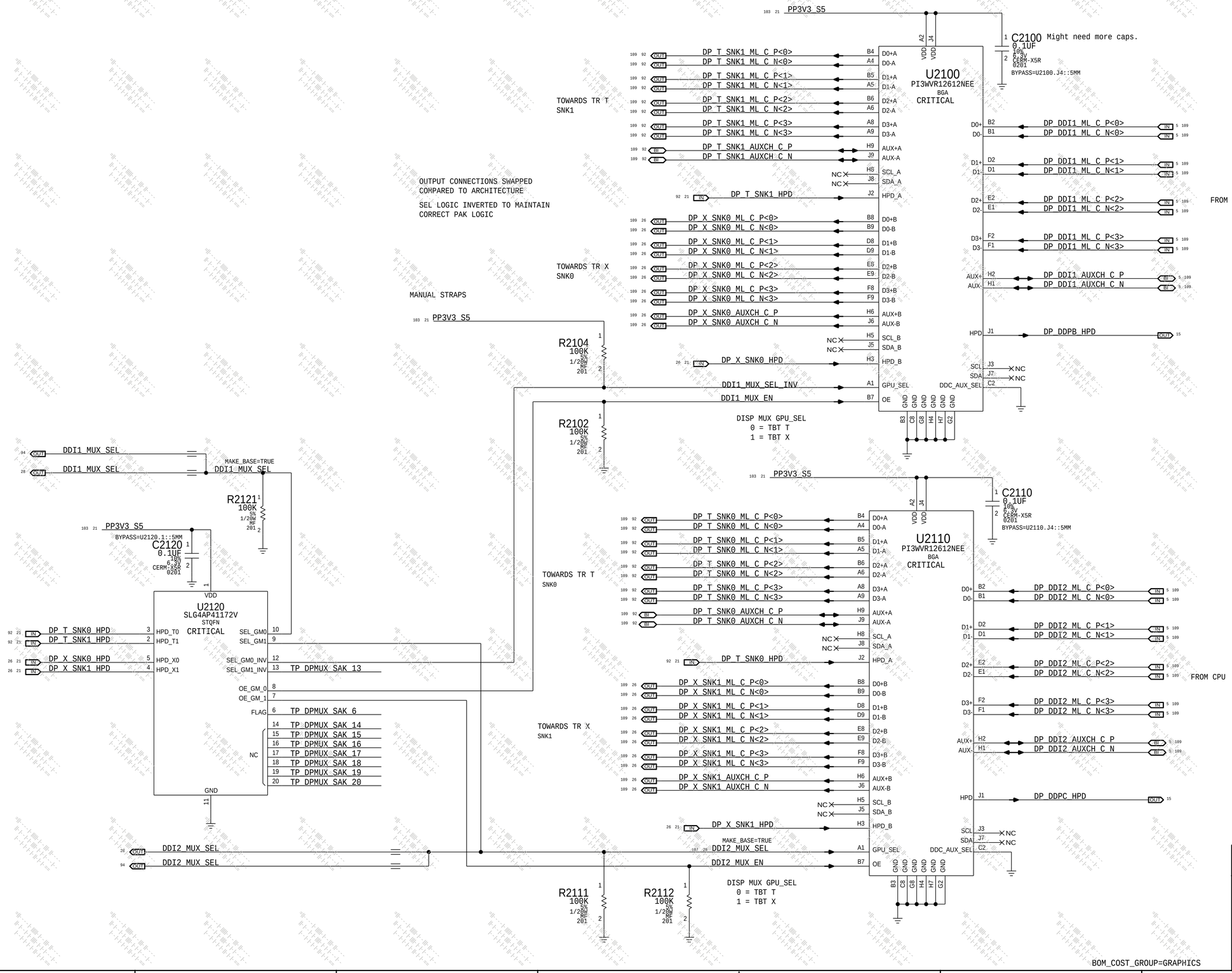

PAGE TITLE: Display Mux

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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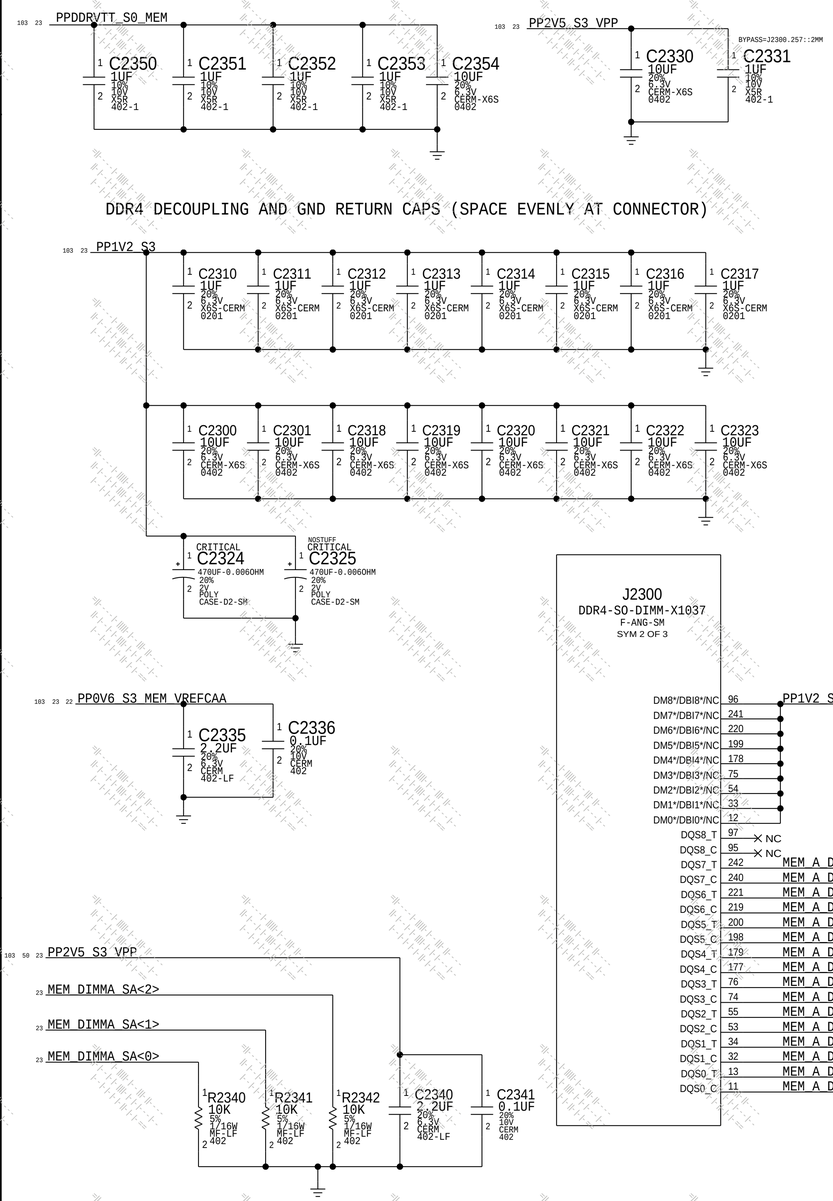
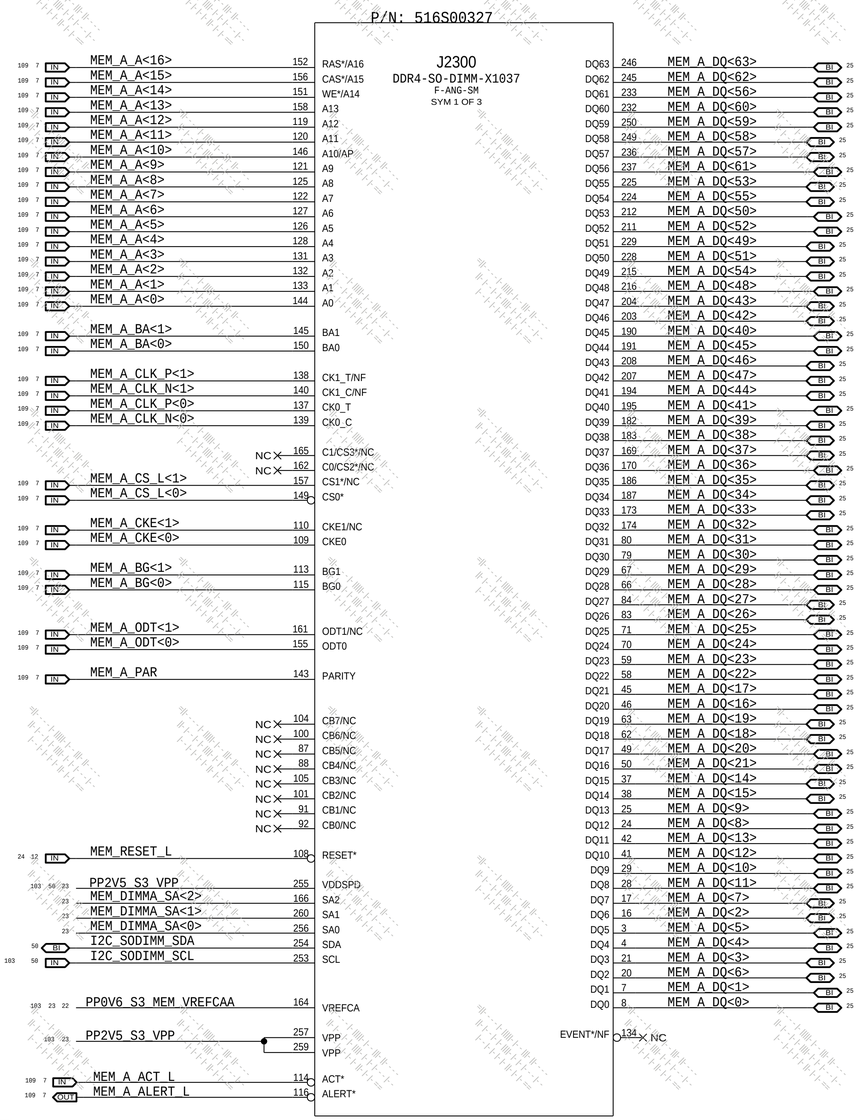
Page Notes

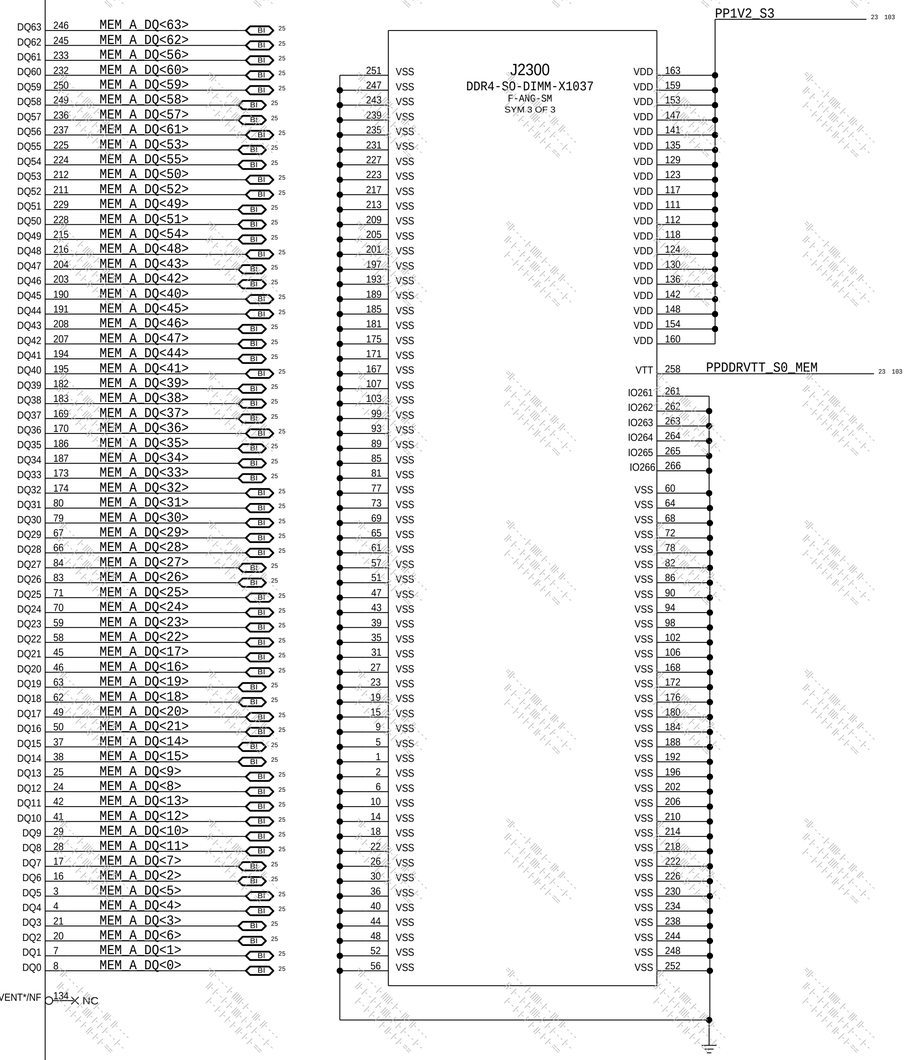
Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PP2V5_S3_MEM_A_SPD (2.5 - 3.3V)

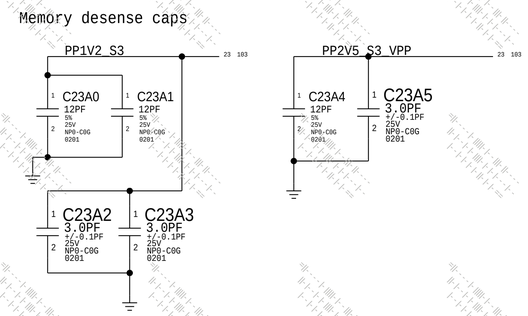
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)









BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: DDR4 DIM A

Apple Inc.

DRAWING NUMBER	051-02424
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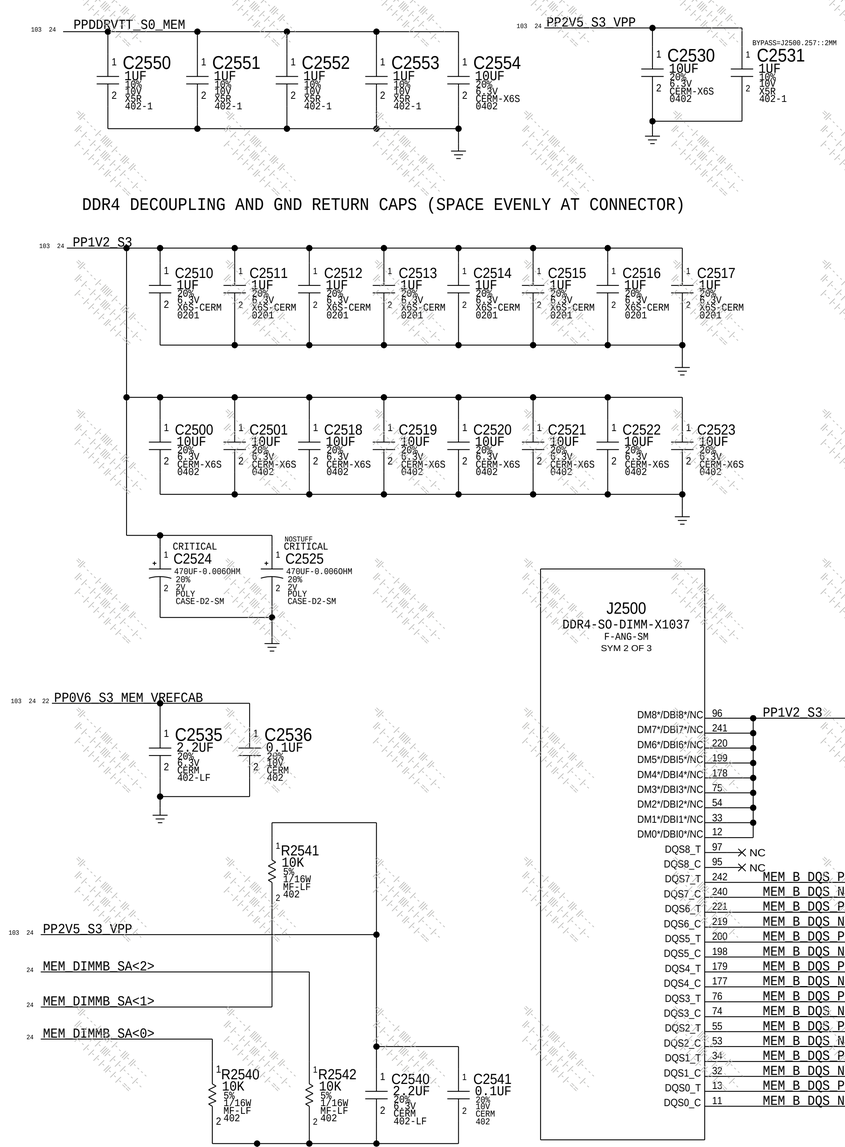
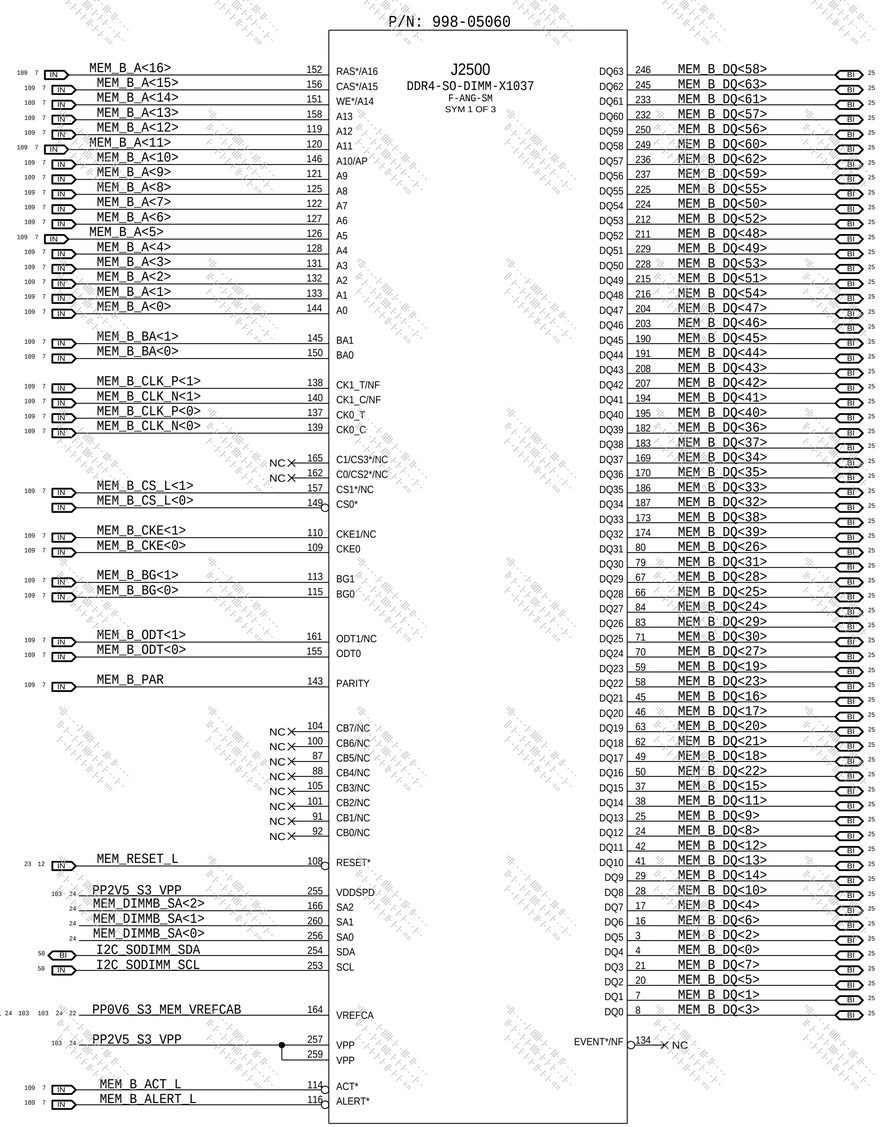
Page Notes

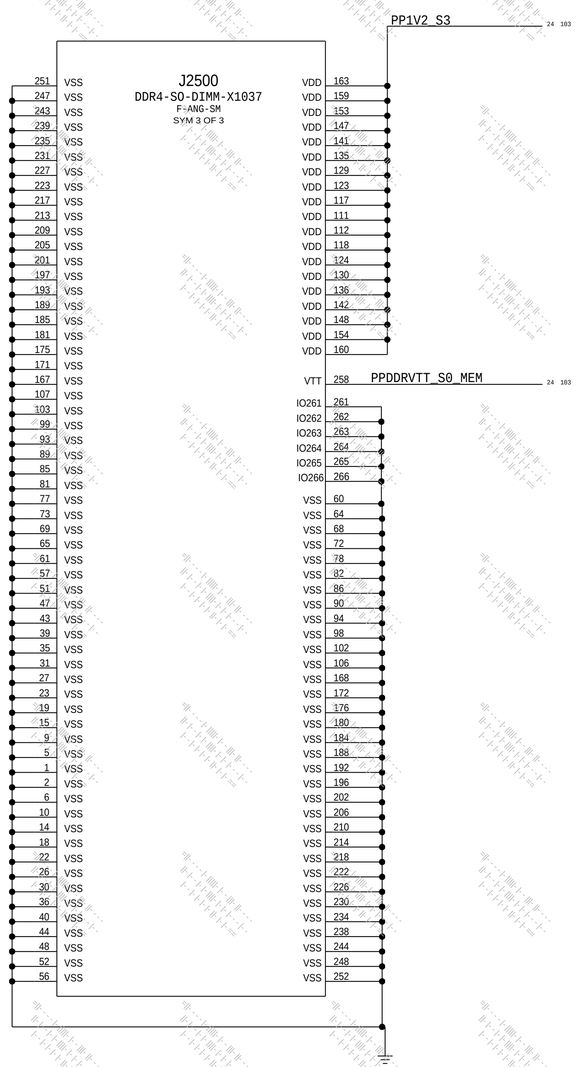
Power aliases required by this page:
- =PPDDRVPP_S3_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP2V5_S3_MEM_B_SPD (2.5 - 3.3V)

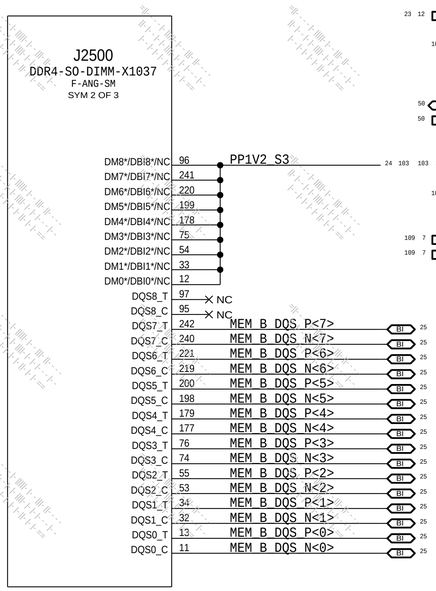
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)









BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	DDR4 DIM B
Apple Inc.	DRAWING NUMBER 051-02424 / SIZE D
	REVISION 6.0.0
	BRANCH dvt-1
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Memory Bit/Byte Swizzle

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BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
DRAM: ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

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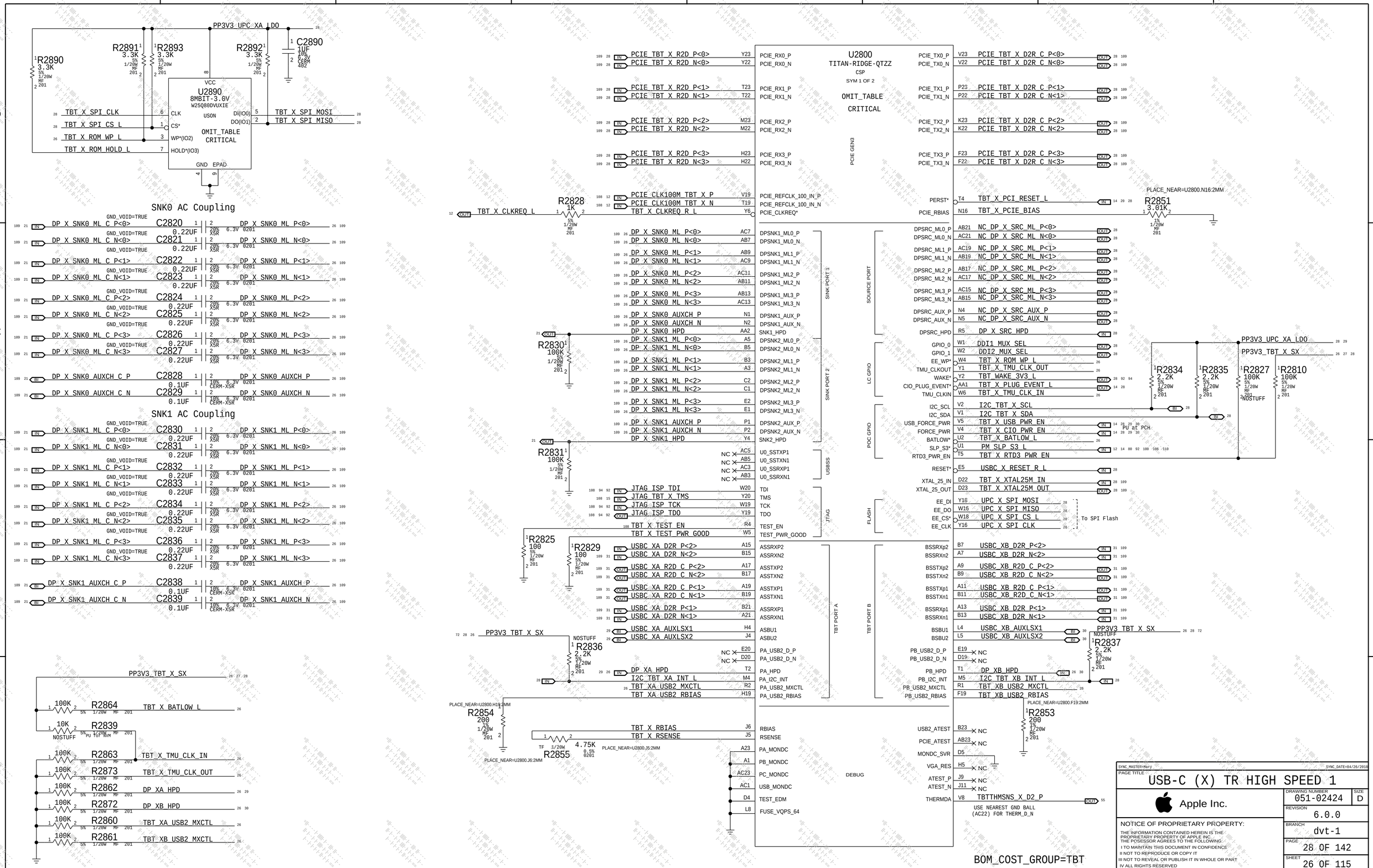

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: USB-C (X) TR HIGH SPEED 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

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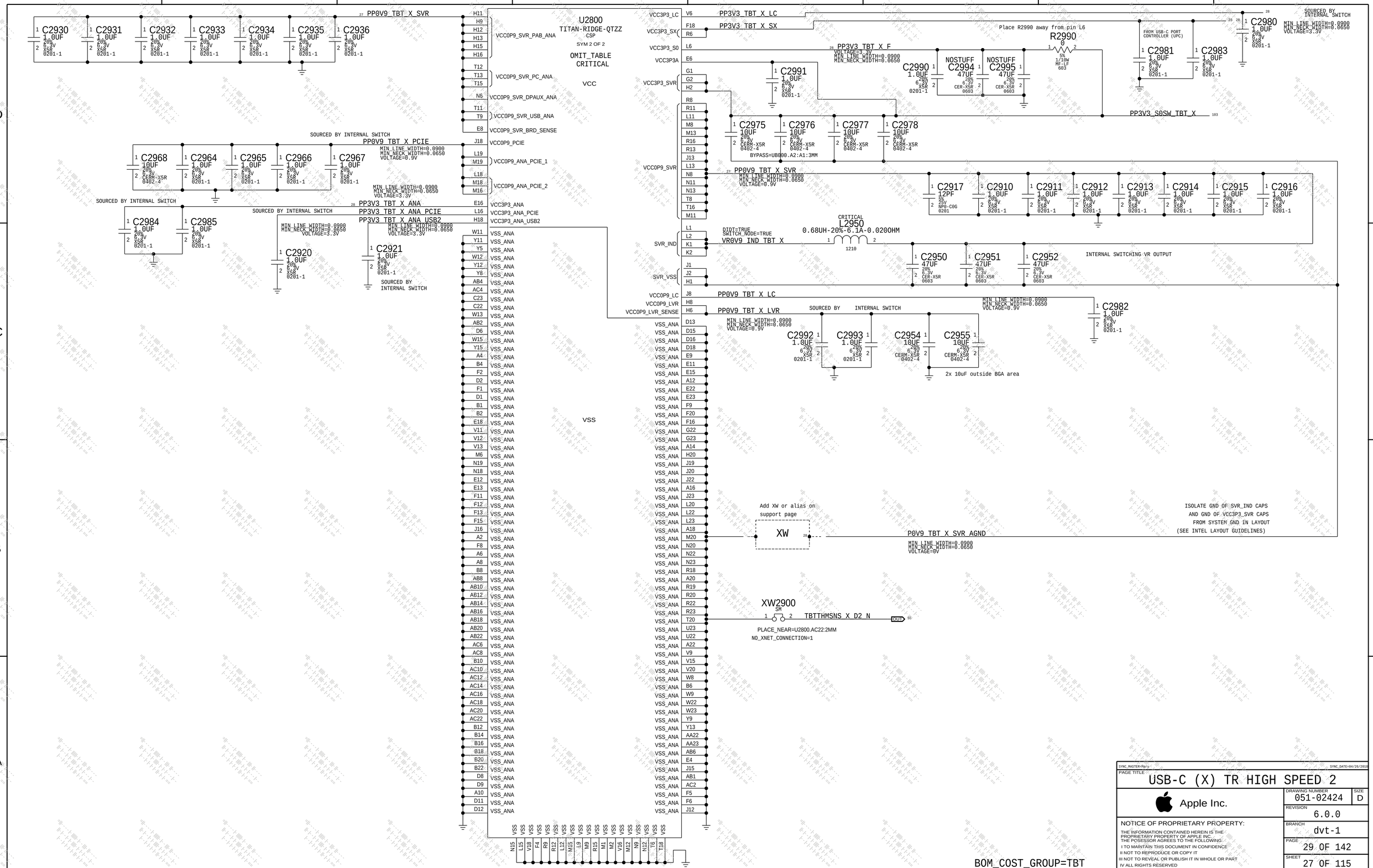

PAGE TITLE: USB-C (X) TR HIGH SPEED 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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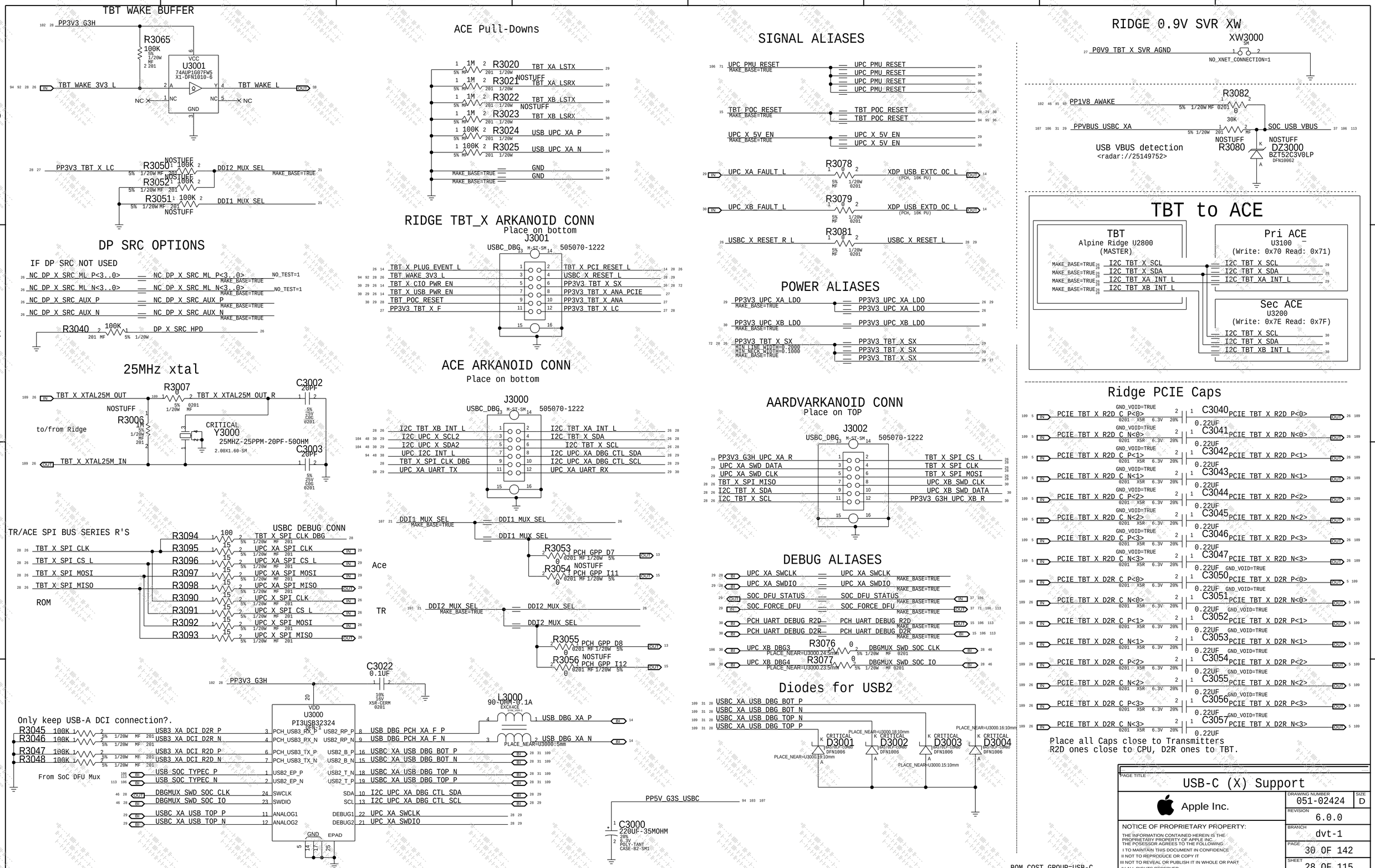
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R3065 100K
U3001 74AUP1G07FW5 X1-DFN1010-6
TBT WAKE 3V3 L
TBT WAKE L
PP3V3 TBT X LC
R3050 100K NOSTUFF
R3052 100K NOSTUFF
R3051 100K NOSTUFF
DDI2 MUX SEL
DDI1 MUX SEL
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ACE Pull-Downs
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R3021 1M NOSTUFF TBT XA LSRX
R3022 1M TBT XB LSTX
R3023 1M NOSTUFF TBT XB LSRX
R3024 100K USB UPC XA P
R3025 100K USB UPC XA N
GND
SIGNAL ALIASES
UPC PMU RESET
TBT POC RESET
UPC X 5V EN
UPC XA FAULT L
UPC XB FAULT L
USBC X RESET R L
R3078 0 XDP USB EXTC OC L
R3079 0 XDP USB EXTD OC L
R3081 0 USBC X RESET L
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SOC USB VBUS
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DZ3000 BZT52C3V0LP
TBT to ACE
TBT
Alpine Ridge U2800
(MASTER)
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I2C TBT X SDA
I2C TBT XA INT L
I2C TBT XB INT L
Pri ACE
U3100
(Write: 0x70 Read: 0x71)
Sec ACE
U3200
(Write: 0x7E Read: 0x7F)
RIDGE TBT_X ARKANOID CONN
Place on bottom
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TBT X PLUG EVENT L
TBT WAKE 3V3 L
TBT X CIO PWR EN
TBT X USB PWR EN
TBT POC RESET
PP3V3 TBT X F
TBT X PCI RESET L
USBC X RESET L
PP3V3 TBT X SX
PP3V3 TBT X ANA PCIE
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PP3V3 TBT X LC
POWER ALIASES
PP3V3 UPC XA LDO
PP3V3 UPC XB LDO
PP3V3 TBT X SX
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
Ridge PCIE Caps
PCIE TBT X R2D C P<0>
PCIE TBT X R2D P<0>
PCIE TBT X R2D C N<0>
PCIE TBT X R2D N<0>
PCIE TBT X R2D C P<1>
PCIE TBT X R2D P<1>
PCIE TBT X R2D C N<1>
PCIE TBT X R2D N<1>
PCIE TBT X R2D C P<2>
PCIE TBT X R2D P<2>
PCIE TBT X R2D C N<2>
PCIE TBT X R2D N<2>
PCIE TBT X R2D C P<3>
PCIE TBT X R2D P<3>
PCIE TBT X R2D C N<3>
PCIE TBT X R2D N<3>
PCIE TBT X D2R C P<0>
PCIE TBT X D2R P<0>
PCIE TBT X D2R C N<0>
PCIE TBT X D2R N<0>
PCIE TBT X D2R C P<1>
PCIE TBT X D2R P<1>
PCIE TBT X D2R C N<1>
PCIE TBT X D2R N<1>
PCIE TBT X D2R C P<2>
PCIE TBT X D2R P<2>
PCIE TBT X D2R C N<2>
PCIE TBT X D2R P<2>
PCIE TBT X D2R C P<3>
PCIE TBT X D2R P<3>
PCIE TBT X D2R C N<3>
PCIE TBT X D2R N<3>
C3040 0.22UF
C3041 0.22UF
C3042 0.22UF
C3043 0.22UF
C3044 0.22UF
C3045 0.22UF
C3046 0.22UF
C3047 0.22UF
C3050 0.22UF
C3051 0.22UF
C3052 0.22UF
C3053 0.22UF
C3054 0.22UF
C3055 0.22UF
C3056 0.22UF
C3057 0.22UF
DP SRC OPTIONS
IF DP SRC NOT USED
NC DP X SRC ML P<3..0>
NC DP X SRC ML N<3..0>
NC DP X SRC AUX P
NC DP X SRC AUX N
NO_TEST=1
R3040 100K DP X SRC HPD
25MHz xtal
TBT X XTAL25M OUT
TBT X XTAL25M OUT R
R3007 0
C3002 20PF
R3006 1M NOSTUFF
to/from Ridge
CRITICAL
Y3000 25MHZ-25PPM-20PF-500HM
2.00X1.60-SM
C3003 20PF
TBT X XTAL25M IN
ACE ARKANOID CONN
Place on bottom
J3000
USBC_DBG 505070-1222
I2C TBT XB INT L
I2C UPC X SCL2
I2C UPC X SDA2
UPC I2C INT L
TBT X SPI CLK DBG
UPC XA UART TX
I2C TBT XA INT L
I2C TBT X SDA
I2C TBT X SCL
I2C UPC XA DBG CTL SDA
I2C UPC XA DBG CTL SCL
UPC XA UART RX
AARDVARKANOID CONN
Place on TOP
J3002
USBC_DBG 505070-1222
PP3V3 G3H UPC XA R
UPC XA SWD DATA
UPC XA SWD CLK
TBT X SPI MISO
I2C TBT X SDA
I2C TBT X SCL
TBT X SPI CS L
TBT X SPI CLK
TBT X SPI MOSI
UPC XB SWD CLK
UPC XB SWD DATA
PP3V3 G3H UPC XB R
DDI1 MUX SEL
R3053 0 PCH GPP D7
R3054 0 NOSTUFF PCH GPP I11
Ace
TR
DDI2 MUX SEL
R3055 0 PCH GPP D8
R3056 0 NOSTUFF PCH GPP I12
TR/ACE SPI BUS SERIES R'S
TBT X SPI CLK
TBT X SPI CS L
TBT X SPI MOSI
TBT X SPI MISO
ROM
R3094 100
R3095 15
R3096 15
R3097 15
R3098 15
R3090 15
R3091 15
R3092 15
R3093 15
TBT X SPI CLK DBG
UPC XA SPI CLK
UPC XA SPI CS L
UPC XA SPI MOSI
UPC XA SPI MISO
UPC X SPI CLK
UPC X SPI CS L
UPC X SPI MOSI
UPC X SPI MISO
USBC DEBUG CONN
DEBUG ALIASES
UPC XA SWCLK
UPC XA SWDIO
SOC DFU STATUS
SOC FORCE DFU
PCH UART DEBUG R2D
PCH UART DEBUG D2R
UPC XB DBG3
UPC XB DBG4
R3076 0 DBGMUX SWD SOC CLK
R3077 0 DBGMUX SWD SOC IO
PLACE_NEAR=U3000.24:5mm
PLACE_NEAR=U3000.23:5mm
C3022 0.1UF
PP3V3 G3H
U3000 PI3USB32324
L3000 90-OHM-0.1A
USB DBG XA P
USB DBG XA N
PLACE_NEAR=U3000:5mm
USB DBG PCH XA F P
USB DBG PCH XA F N
USB3 XA DCI D2R P
USB3 XA DCI D2R N
USB3 XA DCI R2D P
USB3 XA DCI R2D N
USB SOC TYPEC P
USB SOC TYPEC N
DBGMUX SWD SOC CLK
DBGMUX SWD SOC IO
USBC XA USB TOP P
USBC XA USB TOP N
USBC XA USB DBG BOT P
USBC XA USB DBG BOT N
USBC XA USB DBG TOP N
USBC XA USB DBG TOP P
I2C UPC XA DBG CTL SDA
I2C UPC XA DBG CTL SCL
UPC XA SWCLK
UPC XA SWDIO
R3045 100K
R3046 100K
R3047 100K
R3048 100K
From SoC DFU Mux
Only keep USB-A DCI connection?.
Diodes for USB2
USBC XA USB DBG BOT P
USBC XA USB DBG BOT N
USBC XA USB DBG TOP N
USBC XA USB DBG TOP P
D3001 CRITICAL
D3002 CRITICAL
D3003 CRITICAL
D3004 CRITICAL
PLACE_NEAR=U3000.19:10mm
PLACE_NEAR=U3000.18:10mm
PLACE_NEAR=U3000.15:10mm
PLACE_NEAR=U3000.16:10mm
PP5V G3S USBC
C3000 220UF-35MOHM
Place all Caps close to Transmitters
R2D ones close to CPU, D2R ones to TBT.
BOM_COST_GROUP=USB-C
PAGE TITLE
USB-C (X) Support
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 30 OF 142
SHEET 28 OF 115
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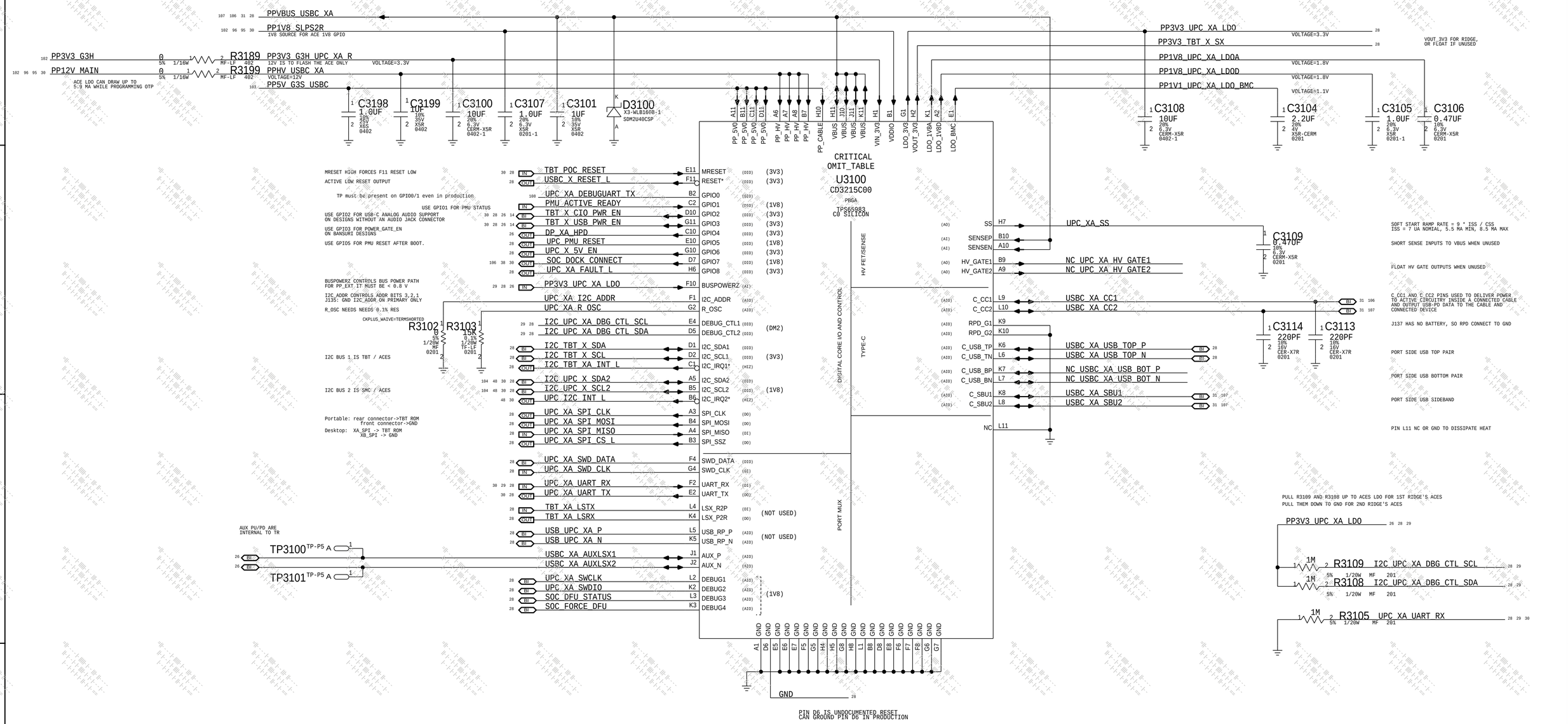
X PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY



NOTE:
DEBUG MUX IS CONNECTED TO
PRIMARY ACE OF 1ST RIDGE (XA ACE)
R3752-R3755, R3790-R3792 ARE OPTIONAL

BOM_COST_GROUP=USB-C

NOT SYNCED TO OTHER PLATFORMS
SYNC_DATE=04/26/2018
Mary

PAGE TITLE	PAGE_TITLE=USB-C (X) PORT CONTROLLER A
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
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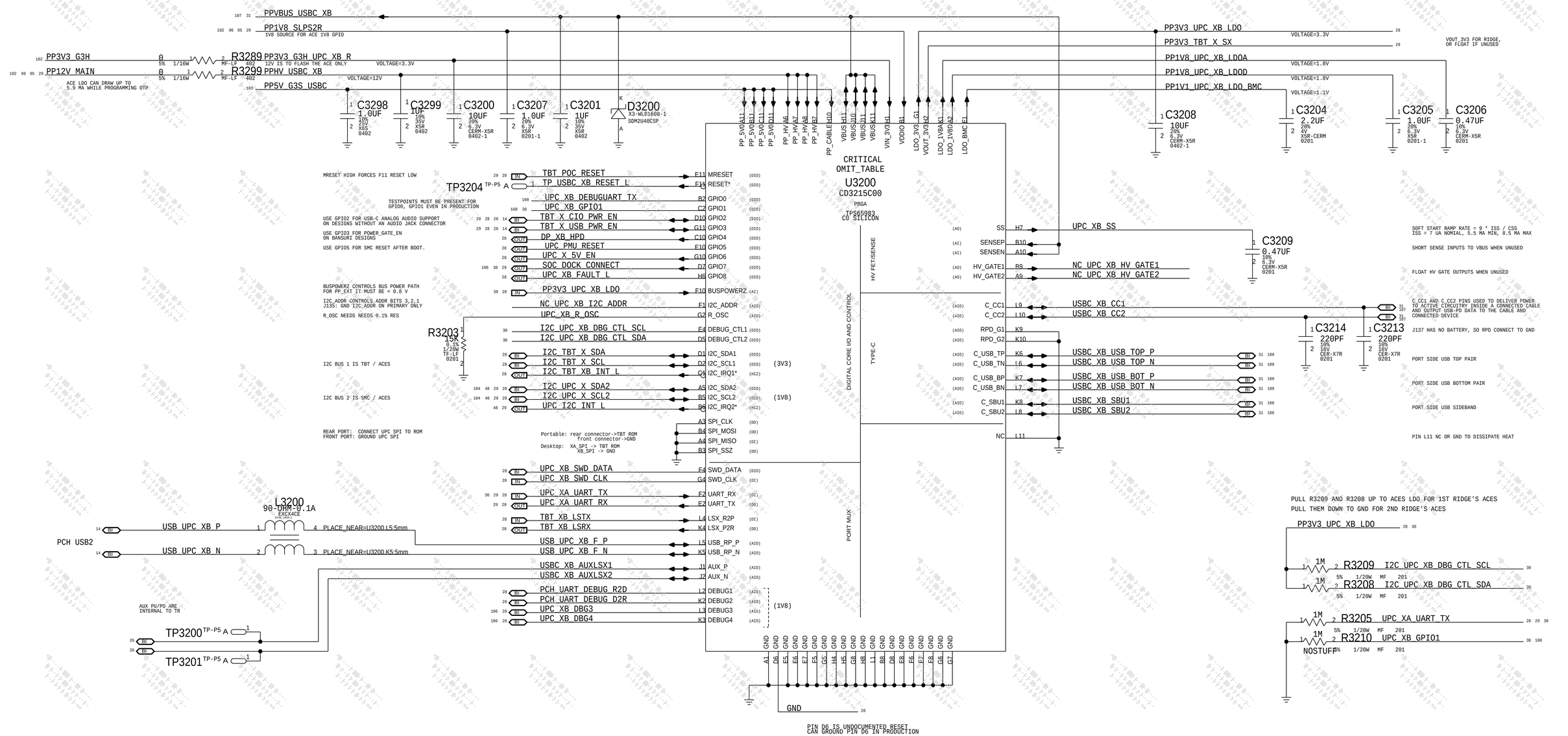
X SECONDARY ACE1 USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

NOT SYNCED TO OTHER PLATFORMS
SYNC_DATE=04/26/2018
Mary

PAGE TITLE	PAGE_TITLE=USB-C (X) PORT CONTROLLER B
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J137 SUPPORTS 5V @ 3A

J137 HAS A QUAD-PACK USB-C CONNECTOR

NOTE: DEBUG MUX 2 (U3000) CONNECTS TO THIS PORT

PLACE VBUS CAPS NEAR EACH VBUS PIN

PPVBUS_USBC_XA
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF C3304 1UF 10% 25V X5R 402

D3300 1610 ESDA25P35-1U1M

C3300 0.01UF 10% 25V X5R-CERM 0201
C3301 0.01UF 10% 25V X5R-CERM 0201
C3302 0.01UF 10% 25V X5R-CERM 0201
C3303 0.01UF 10% 25V X5R-CERM 0201
C3310 1UF 10% 25V X5R 402
C3306 0.01UF 10% 25V X5R-CERM 0201
C3307 0.01UF 10% 25V X5R-CERM 0201
C3308 0.01UF 10% 25V X5R-CERM 0201
C3309 0.01UF 10% 25V X5R-CERM 0201
C3311 3PF +/-0.1PF 25V C0G 0201
C3312 12PF 5% 50V C0G-CERM 0201

USBC_XA_D2R_P<2> — R3370 3.01 1% 1/20W MF 0201 — USBC_XA_D2R_RC_P<2> — C3370 0.33UF 25V 10% CER-X5R 0201 — USBC_XA_D2R_CONN_P<2>
USBC_XA_D2R_N<2> — R3371 3.01 1% 1/20W MF 0201 — USBC_XA_D2R_RC_N<2> — C3371 0.33UF 25V 10% CER-X5R 0201 — USBC_XA_D2R_CONN_N<2>
USBC_XA_SBU1
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_TOP_P
USBC_XA_CC1
USBC_XA_R2D_C_N<1> — R3372 3.01 1% 1/20W MF 0201 — USBC_XA_R2D_RC_N<1> — C3372 0.22UF 25V 10% X5R 0201 — USBC_XA_R2D_CONN_N<1>
USBC_XA_R2D_C_P<1> — R3373 3.01 1% 1/20W MF 0201 — USBC_XA_R2D_RC_P<1> — C3373 0.22UF 25V 10% X5R 0201 — USBC_XA_R2D_CONN_P<1>

CRITICAL J3300 — RCPT-USBC-QUAD-X1037 F-RT-TH — SYM 1 OF 5 CONN A

USBC_XA_D2R_CONN_P<1>
USBC_XA_D2R_CONN_N<1>
USBC_XA_R2D_CONN_N<2>
USBC_XA_R2D_CONN_P<2>

C3378 0.33UF — USBC_XA_D2R_RC_P<1> — R3378 3.01 — USBC_XA_D2R_P<1>
C3379 0.33UF — USBC_XA_D2R_RC_N<1> — R3379 3.01 — USBC_XA_D2R_N<1>
USBC_XA_SBU2
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_CC2
C3380 0.22UF — USBC_XA_R2D_RC_N<2> — R3380 3.01 — USBC_XA_R2D_C_N<2>
C3381 0.22UF — USBC_XA_R2D_RC_P<2> — R3381 3.01 — USBC_XA_R2D_C_P<2>

DZ3300 SESDL2011 DSN2-THICKSTNCL; DZ3301; DZ3304; DZ3305; DZ3390 5V-6.2PF 0201-THICKSTNCL; DZ3302 ESD8011 X3DFN2-THICKSTNCL; DZ3303; DZ3391; DZ3392; DZ3308; DZ3309; DZ3393; DZ3306; DZ3307; DZ3310; DZ3311

R3301 220K; R3300; R3303; R3302; R3305; R3304; R3307; R3306

PPVBUS_USBC_XB
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF C3354 1UF 10% 25V X5R 402

D3370 1610 ESDA25P35-1U1M

C3350 0.01UF 10% 25V X5R-CERM 0201
C3351 0.01UF 10% 25V X5R-CERM 0201
C3352 0.01UF 10% 25V X5R-CERM 0201
C3353 0.01UF 10% 25V X5R-CERM 0201
C3360 1UF 10% 25V X5R 402
C3356 0.01UF 10% 25V X5R-CERM 0201
C3357 0.01UF 10% 25V X5R-CERM 0201
C3358 0.01UF 10% 25V X5R-CERM 0201
C3359 0.01UF 10% 25V X5R-CERM 0201
C3361 3PF +/-0.1PF 25V C0G 0201
C3362 12PF 5% 50V C0G-CERM 0201

USBC_XB_D2R_P<2> — R3374 3.01 1% 1/20W MF 0201 — USBC_XB_D2R_RC_P<2> — C3374 0.33UF 25V 10% CER-X5R 0201 — USBC_XB_D2R_CONN_P<2>
USBC_XB_D2R_N<2> — R3375 3.01 1% 1/20W MF 0201 — USBC_XB_D2R_RC_N<2> — C3375 0.33UF 25V 10% CER-X5R 0201 — USBC_XB_D2R_CONN_N<2>
USBC_XB_SBU1
USBC_XB_USB_TOP_N
USBC_XB_USB_TOP_P
USBC_XB_CC1
USBC_XB_R2D_C_N<1> — R3376 3.01 1% 1/20W MF 0201 — USBC_XB_R2D_RC_N<1> — C3376 0.22UF 25V 10% X5R 0201 — USBC_XB_R2D_CONN_N<1>
USBC_XB_R2D_C_P<1> — R3377 3.01 1% 1/20W MF 0201 — USBC_XB_R2D_RC_P<1> — C3377 0.22UF 25V 10% X5R 0201 — USBC_XB_R2D_CONN_P<1>

CRITICAL J3300 — RCPT-USBC-QUAD-X1037 F-RT-TH — SYM 2 OF 5 CONN B

USBC_XB_D2R_CONN_P<1>
USBC_XB_D2R_CONN_N<1>
USBC_XB_R2D_CONN_N<2>
USBC_XB_R2D_CONN_P<2>

C3382 0.33UF — USBC_XB_D2R_RC_P<1> — R3382 3.01 — USBC_XB_D2R_P<1>
C3383 0.33UF — USBC_XB_D2R_RC_N<1> — R3383 3.01 — USBC_XB_D2R_N<1>
USBC_XB_SBU2
USBC_XB_USB_BOT_N
USBC_XB_USB_BOT_P
USBC_XB_CC2
C3384 0.22UF — USBC_XB_R2D_RC_N<2> — R3384 3.01 — USBC_XB_R2D_C_N<2>
C3385 0.22UF — USBC_XB_R2D_RC_P<2> — R3385 3.01 — USBC_XB_R2D_C_P<2>

DZ3320 SESDL2011 DSN2-THICKSTNCL; DZ3321; DZ3324; DZ3325; DZ3394 5V-6.2PF 0201-THICKSTNCL; DZ3322 ESD8011 X3DFN2-THICKSTNCL; DZ3323; DZ3395; DZ3396; DZ3328; DZ3329; DZ3397; DZ3326; DZ3327; DZ3330; DZ3331

R3309 220K; R3308; R3311; R3310; R3313; R3312; R3315; R3314

BOM_COST_GROUP=USB-C

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: USB-C (X) CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 33 OF 142
SHEET: 31 OF 115

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PLACE HOLDER

BOM_COST_GROUP=DEBUG

SYNC_MASTER=ARCT SYNC_DATE=04/26/2018

PAGE TITLE

Empty

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SYNC_MASTER=ARCT SYNC_DATE=04/26/2018

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Software	I2S_SEL	UART_SEL	UART I/F
Gen1 (macOS)	0	1	UART (PCH)
Gen2	X	0	UART (SOC)

BT_DEV_WAKE option

36 35 OUT BT_DEV_WAKE — R3601 1 0 2 5% 1/20W MF 0201 — SOC_BT_DEV_WAKE IN 38

R3602 1 0 2 5% 1/20W MF 0201 NOSTUFF — PCH_BT_DEV_WAKE IN 15

107 103 35 34 PP1V8_G3S — R3621 1 100K 5% 1/20W MF 201 2

MAKE_BASE=TRUE

39 IN UART_BT_LH_R2D — UART_BT_LH_R2D OUT 35 36

39 OUT UART_BT_LH_D2R — UART_BT_LH_D2R IN 35 36

MAKE_BASE=TRUE

38 34 BTUARTMUX_SEL_PCH — R3660 1 100K 5% 1/20W MF 201 2

Q3660
DMN32D1LFB4
DFN1006

108 106 45 12 IN PM_PCH_PWROK — 1 G D S 3 2

APN376S00335
min Vgs(th)0.7V

Q3660 ensures BT does
not backpower the PCH

107 103 35 34 PP1V8_G3S — R3641 1 0 5% 1/20W MF 0201 2

103 34 PP3V3_G3S_WLANBT

BYPASS=U3640::5mm
C3640 1 0.1UF 10% 16V X5R-CERM 0201 2

39 IN UART_BT_R2D — 5 M+

39 OUT UART_BT_D2R — 4 M-

15 IN PCH_BT_UART_R2D — 7 D+

15 OUT PCH_BT_UART_D2R — 6 D-

BTUARTMUX_OE_L — 8 OE*

9 VCC

U3640
PI3USB102J
X2QFN
CRITICAL

3 GND

1 Y+ UART_BT_MUX_R2D — OUT 35 36

2 Y- UART_BT_MUX_D2R — IN 35 36

SEL 10 BTUARTMUX_SEL_PCH — IN 34 38

SEL	OUTPUT
L	SOC (M)
H	PCH (D)

107 103 35 34 PP1V8_G3S — R3651 1 100K 5% 1/20W MF 201 2

103 34 PP3V3_G3S_WLANBT

BYPASS=U3650::5mm
C3650 1 0.1UF 10% 16V X5R-CERM 0201 2

39 IN UART_BT_R2D_RTS_L — 5 M+

39 OUT UART_BT_D2R_CTS_L — 4 M-

15 IN PCH_BT_UART_RTS_L — 7 D+

15 OUT PCH_BT_UART_CTS_L — 6 D-

BTUARTMUX_OE_L — 8 OE*

9 VCC

U3650
PI3USB102J
X2QFN
CRITICAL

3 GND

1 Y+ UART_BT_MUX_CTS_L — OUT 35 36

2 Y- UART_BT_MUX_RTS_L — IN 35 36

SEL 10 BTUARTMUX_SEL_PCH — 34 38

SEL	OUTPUT
L	SOC (M)
H	PCH (D)

SOC AND PCH RTS GO TO HPN CTS
SOC AND PCH CTS GO TO HPN RTS

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
WIFI/BT: Support

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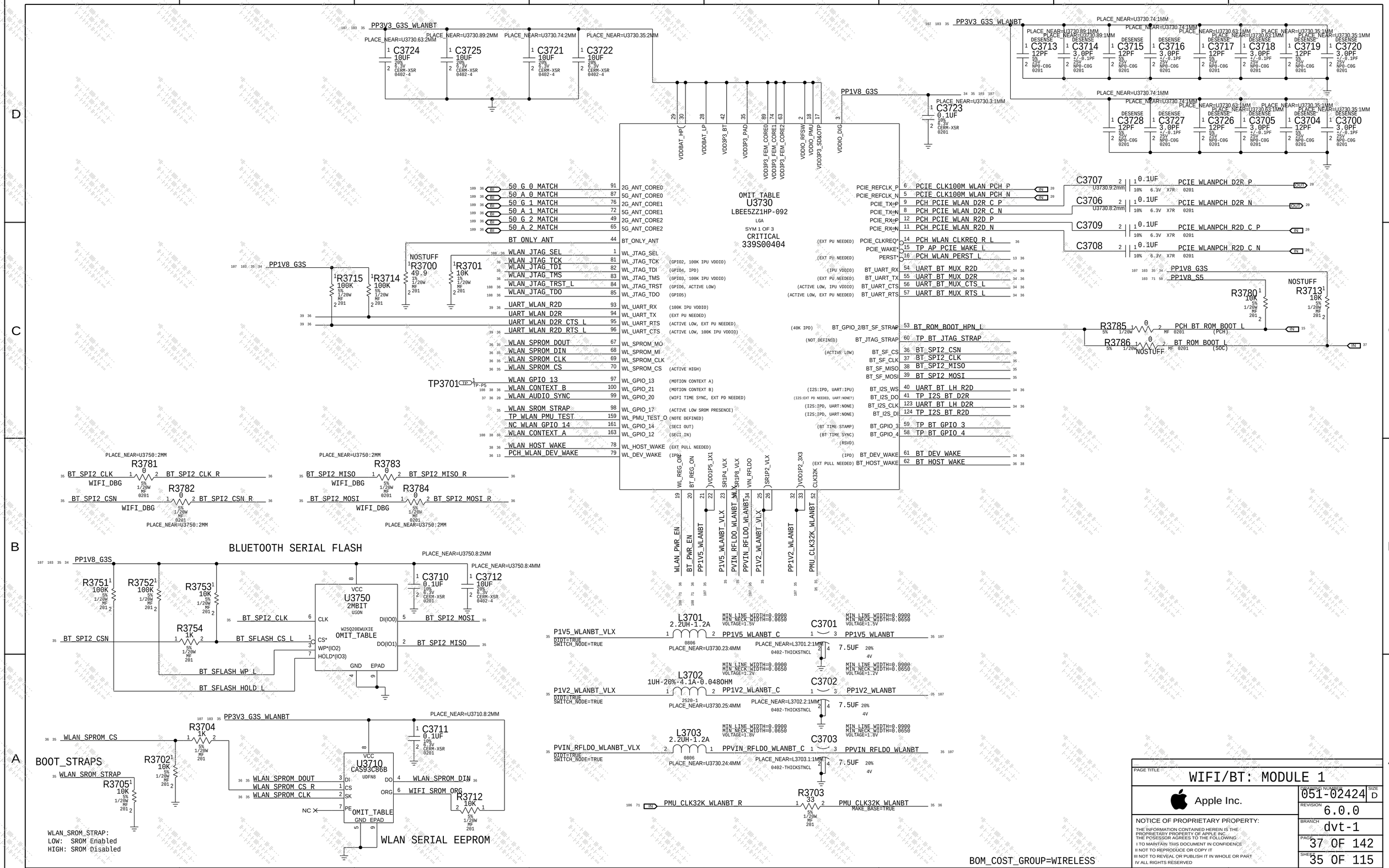

PAGE TITLE
WIFI/BT: MODULE 1

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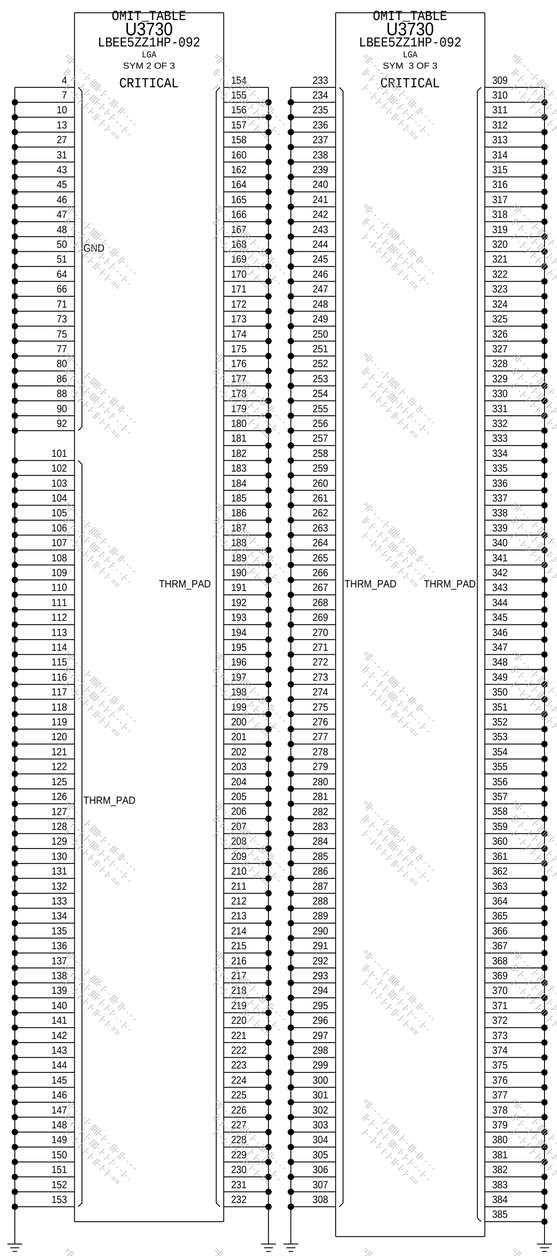
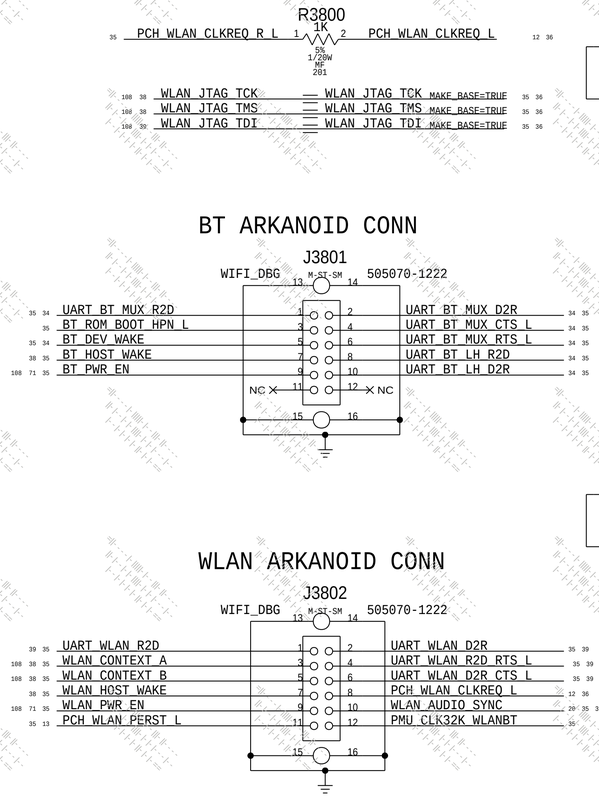
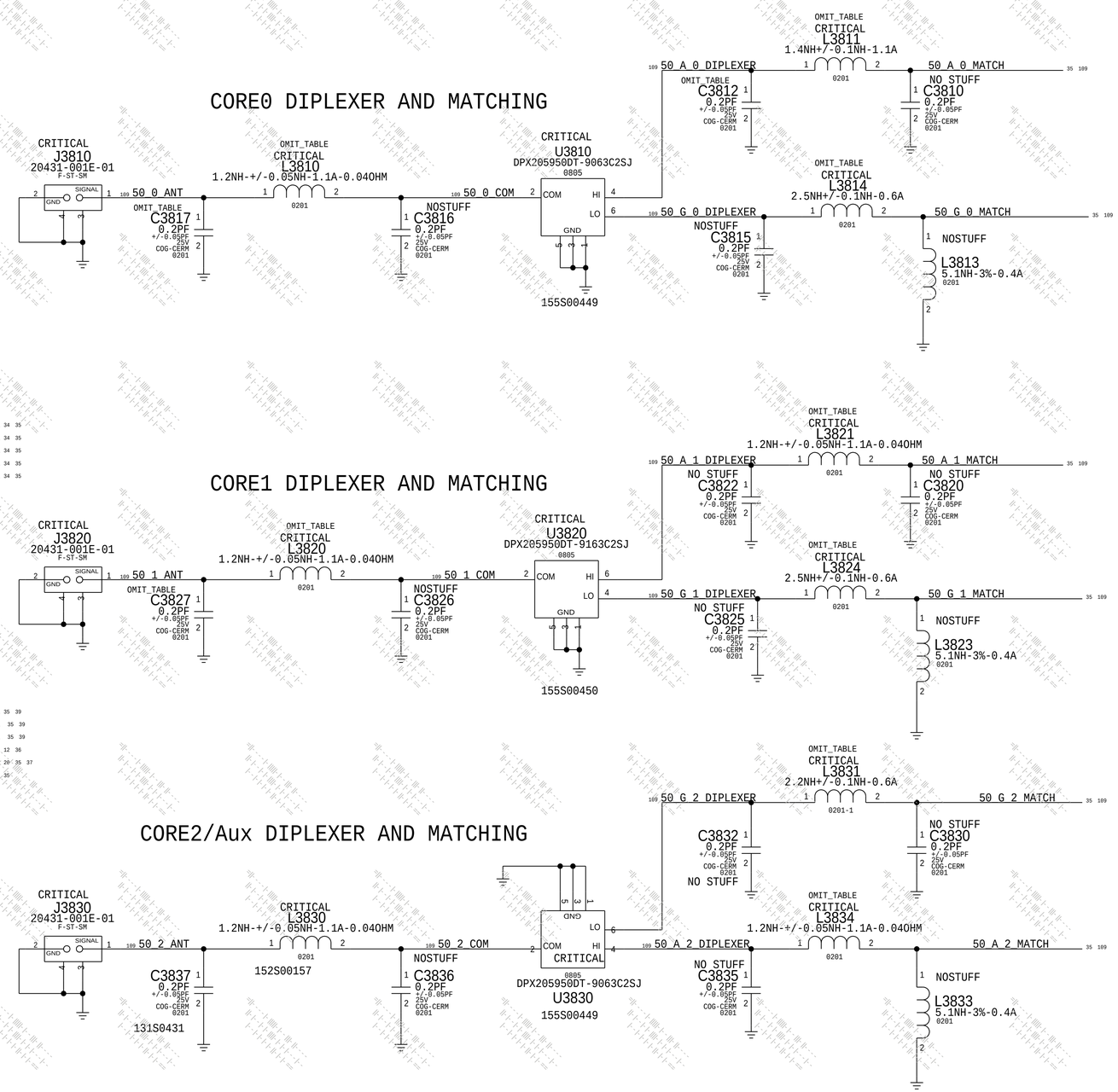
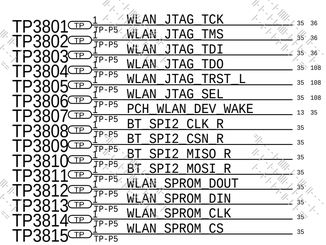
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00152	1	IND,0.9NH,1,1A,0201	L3810	CRITICAL	
131S0631	1	CAP,CER,0.3pF,0201	C3817,C3827	CRITICAL	
152S00153	1	IND,1NH,1,1A,0201	L3820	CRITICAL	
152S1222	1	IND,3NH,1,1A,0201	C3812	CRITICAL	
131S0555	1	cap,CER,1pF,0201	L3811	CRITICAL	









PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	5	RES,MF,0 OHM,0.5%,0201	L3814,L3821,L3824,L3831,L3834	CRITICAL	

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: MODULE 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 38 OF 142
SHEET 36 OF 115

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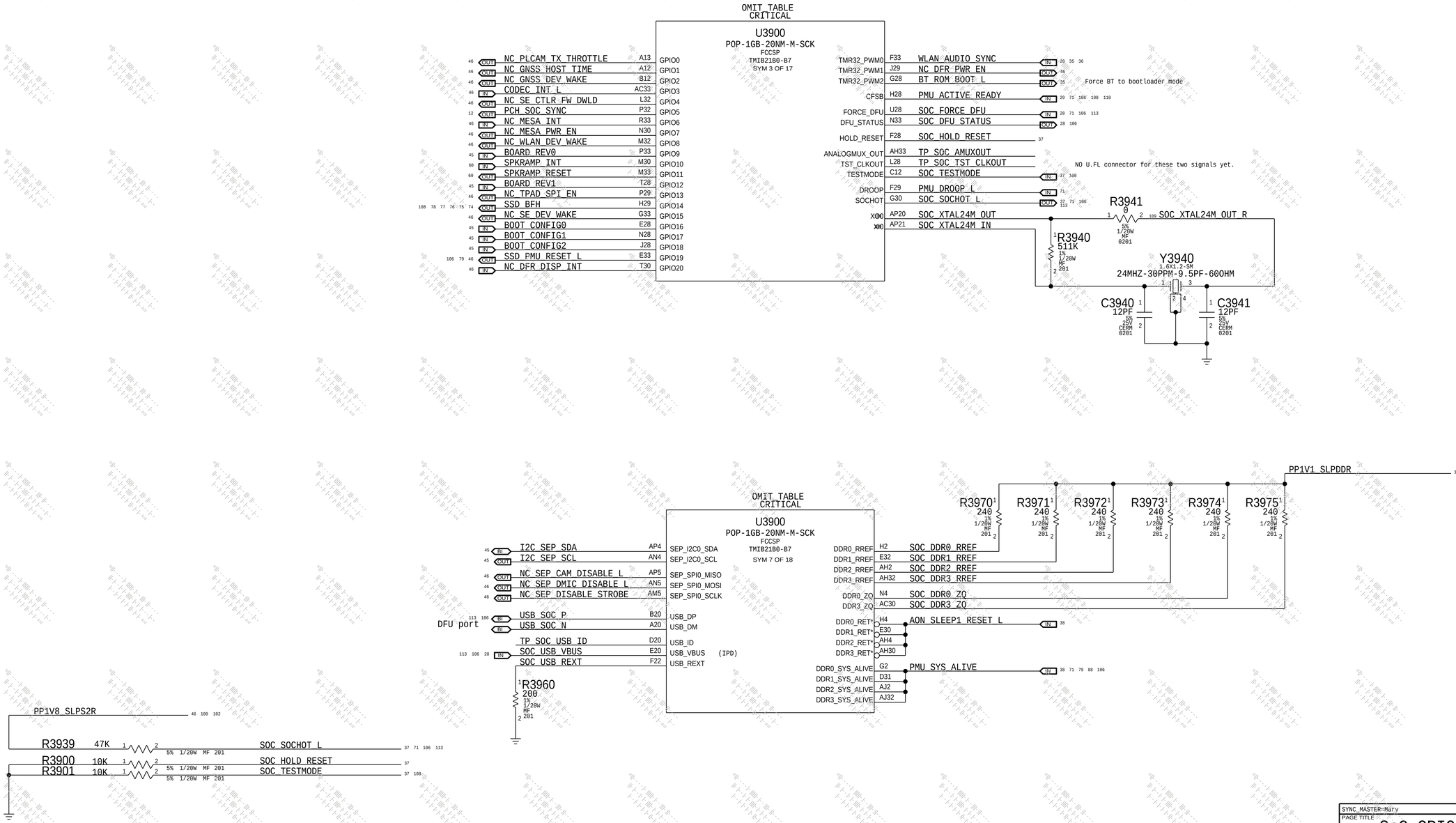
Note 1) IPU represents SW configured state, not HW default



BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC GPIO/SEP/USB/DDR/Test

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 6 OF 17

108 36 35	OUT	WLAN_CONTEXT_A	B5	AOP_FUNC[0]		AOP_PDM_CLK0	N6	NC_PDM_DMIC_CLK0_R	OUT	46
108 36 35	OUT	WLAN_CONTEXT_B	D4	AOP_FUNC[1]		AOP_PDM_CLK1	J6	NC_PDM_DMIC_CLK1_R	OUT	46
46	IN	NC_GYRO_INT1	G1	AOP_FUNC[2]	(IPD)	AOP_PDM_CLK2 (IPU)	F5	SMC_FIXTURE_MODE_L	IN	TP is needed on Dev_Supply
46	IN	NC_GYRO_INT2	C5	AOP_FUNC[3]	(IPD)	AOP_PDM_CLK3 (IPU)	F2	NC_PLCAM_PROX_INT_L	IN	46
34	OUT	BTUARTMUX_SEL_PCH	D1	AOP_FUNC[4]		AOP_PDM_CLK4	J4	NC_PLCAM_ROMEO_B2B_DETECT	IN	46
15	IN	SOC_PERST_L	E4	AOP_FUNC[5]						
46	IN	NC_ALTIMETER_INT	C4	AOP_FUNC[6]	(IPD)	AOP_PDM_DATA0 (IPD)	F1	NC_PDM_DMIC_DATA0	IN	46
46	OUT	NC_SPI_GYRO_CS_L	F4	AOP_FUNC[7]		AOP_PDM_DATA1 (IPD)	J1	NC_PDM_DMIC_DATA1	IN	46
46	OUT	NC_SPI_ALTIMETER_CS_L	E1	AOP_FUNC[8]						
						AOP_SPI_MOSI	A5	NC_SPI_AOP_SENSOR_MOSI_R	OUT	46
48	OUT	NC_I2C_AOP_SCL	H6	AOP_I2C0_SCL		AOP_SPI_SCLK	E5	NC_SPI_AOP_SENSOR_CLK_R	OUT	46
48	BI	NC_I2C_AOP_SDA	G6	AOP_I2C0_SDA		AOP_SPI_MISO	C2	NC_SPI_AOP_SENSOR_MISO	IN	46

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
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SYM 5 OF 17

46	IN	NC_DFR_TOUCH_INT_L	AG6	AON_GPIO0		JTAG_TCK (IPU)	AF6	SWD_SOC_SWCLK	IN	46 108 113
20	IN	CPU_SMC_THRMTRIP_L	AB6	AON_GPIO1		JTAG_TMS (IPU)	AH1	SWD_SOC_SWDIO	BI	46 108 113
46	IN	NC_SMC_GFX_SELF_THROTTLE	AL1	AON_GPIO2	(IPD)	JTAG_TDI (IPU)	AE6	DEBUG_JTAG_SOC_TDI		106 113
46	OUT	NC_SMC_TOPBLK_SWP_L	AH5	AON_GPIO3		JTAG_TDO	AK1	DEBUG_JTAG_SOC_TDO		106 113
18	IN	XDP_PRESENT_L	AG1	AON_GPIO4		(IPD) JTAG_TRST*	AH6	TP_JTAG_SOC_TRST_L		106
46	OUT	CODEC_RESET_L	AL4	AON_GPIO5		JTAG_SEL	Y8	SOC_JTAG_SEL (DAP=0, TAP=1)		38 108
34	OUT	SOC_BT_DEV_WAKE	AK4	AON_GPIO6						
84	IN	PCIEDN_WAKE_L	AD6	AON_GPIO7	(IPU)	DOCK_CONNECT	AJ5	SOC_DOCK_CONNECT	IN	29 30 38 106
81 20	OUT	ENET_LOW_PWR	AM1	AON_GPIO8						
100	IN	TPAD_SPI_INT_L_ACDC_ID	AJ6	AON_GPIO9		(IPU) AON_SWD0_TMS	AF2	WLAN_JTAG_TMS	BI	36 108
46	IN	NC_SDCONN_STATE_CHANGE_L	AK5	AON_GPIO10	(IPU)	AON_SWD1_TMS	AE4	NC_MESA_MENUKEY_L	IN	46
84	IN	ENET_MEDIA_SENSE	AJ1	AON_GPIO11	(IPD)	AON_SWD01_TCK	AE5	WLAN_JTAG_TCK	OUT	36 108
71	IN	PMU_INT_L	AL6	AON_GPIO12	(IPU)	WDOG	AF5	SOC_WDOG	OUT	71 106
						AON_SLEEP1_RESET*	AC6	AON_SLEEP1_RESET_L	OUT	37
		SPMI_CLK_R	AA6	AON_SPMI_SCLK						
		SPMI_DATA_R	AK2	AON_SPMI_SDATA						
106 71	IN	PMU_CLK32K_SOC	AK6	RT_CLK32768						
		SOC_COLD_RESET_L	AG4	COLD_RESET*						
			AF4	CFSB_AON						
108 106 71	IN	PMU_COLD_RESET_L								

PLACE_NEAR=U3900.AA6:5MM
PLACE_NEAR=U7800.M7:5MM

71 OUT SPMI_CLK — R4036 20 1 2 5% 1/20W MF 201
71 BI SPMI_DATA — R4037 20 1 2 5% 1/20W MF 201

R4039 1 2 4.7K 5% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
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PLACE_NEAR=U3900.B4:5MM
PLACE_NEAR=U3900.R1:5MM
PLACE_NEAR=U3900.T5:5MM
PLACE_NEAR=U3900.T6:5MM

113 109 38 12	BI	ESPI_IO<0> — R4050 20 1 2 5% 1/20W MF 201	109	ESPI_IO_R<0>	R4	SMC_ESPI_IO0		SMC_GPIO0	V4	CODEC_WAKE_L	IN	46
113 109 38 12	BI	ESPI_IO<1> — R4051 20 1 2 5% 1/20W MF 201	109	ESPI_IO_R<1>	R1	SMC_ESPI_IO1		SMC_GPIO1 (IPD)	V8	BT_HOST_WAKE	IN	35 36
113 109 38 12	BI	ESPI_IO<2> — R4052 20 1 2 5% 1/20W MF 201	109	ESPI_IO_R<2>	T5	SMC_ESPI_IO2		SMC_GPIO2 (IPD)	V6	WLAN_HOST_WAKE	IN	35 36
113 109 38 12	BI	ESPI_IO<3> — R4053 20 1 2 5% 1/20W MF 201	109	ESPI_IO_R<3>	T6	SMC_ESPI_IO3		SMC_GPIO3	U4	SMC_GFX_THROTTLE_L	OUT	46
113 109 12	IN	ESPI_CLK	P2	SMC_ESPI_CLK	(IPD)	SMC_GPIO4	V7	LIDINT_L_UARTHDD_D2R	IN	46
113 38 12	IN	ESPI_CS_L	T4	SMC_ESPI_CS*		SMC_GPIO5	U6	PCC_EVENT	BI	108
113 12	IN	ESPI_RESET_L	T2	SMC_ESPI_RESET*	(IPD)	SMC_GPIO6	V1	DP2HDMI_AOP_VDD12ON	IN	46
						SMC_GPIO7	W5	PSU11VOC_WAKE_L	IN	55
46 45	IN	SMC_PECI_RX	M6	SMC_PECI_IN	(IPD)	SMC_GPIO8	AC1	LIDOPEN_PSU12VPGOOD_ACDCBURST_L	BI	100 108
45	OUT	SMC_PECI_TX	R6	SMC_PECI_OUT		SMC_GPIO9	AB2	NC_SPI_DESCRIPTOR_OVERRIDE_L	OUT	46
108 45	OUT	SMC_PCH_PWROK	U7	PCH_PWROK		(IPU) SMC_GPIO10	AB1	NC_DISP_GCON_INT_L	IN	46
108 45	OUT	SMC_PCH_SYS_PWROK	U8	SYS_PWROK		SMC_GPIO11	AA4	PCH_GCON_INT_L		15
						SMC_GPIO12	W8	PSU_P12V_EN_L	OUT	46
45	OUT	SMC_RSMRST_L	U1	RSMRST*		(IPU) SMC_GPIO13	AA1	TBT_WAKE_L	IN	28
108 106 45	OUT	SMC_SYSRST_L	U5	SYS_RESET*		(IPU) SMC_GPIO14	AC2	UPC_I2C_INT_L	IN	28 48 94
106 100 71 12	IN	PM_SLP_S0_L	W1	SLP_S0B		SMC_GPIO_15	K2	TP_SMC_DEBUG	IN	46
63 46 45	BI	SMC_PROCHOT_L	P6	PROCHOT*						
106 88 79 71 37	IN	PMU_SYS_ALIVE	W6	SYS_ALIVE						
						SMC_ADC0	AE1	SMC_P12VIN_VSENSE	IN	46
106 48	OUT	I2C_UPC_SCL	K4	SMC_I2C0_SCL		SMC_ADC1	Y5	SMC_P12VIN_ISENSE	IN	46
106 48	BI	I2C_UPC_SDA	H1	SMC_I2C0_SDA		SMC_ADC2	AE2	SMC_CPU_HI_ISENSE	IN	46
						SMC_ADC3	AB5	SMC_CPU_VCC_ISENSE	IN	46
48	OUT	NC_I2C_SNS0_S0_SCL	L4	SMC_I2C1_SCL		SMC_ADC4	Y7	SMC_CPU_VCC_VSENSE	IN	46
48	BI	NC_I2C_SNS0_S0_SDA	L5	SMC_I2C1_SDA		SMC_ADC5	AD4	SMC_CPUGT_VSENSE	IN	46
						SMC_ADC6	AF1	SMC_CPUGT_ISENSE	IN	46
48	OUT	I2C_SNS1_S0_SCL	M4	SMC_I2C2_SCL		SMC_ADC7	Y6	SMC_P1V2_ISENSE	IN	46
48	BI	I2C_SNS1_S0_SDA	K1	SMC_I2C2_SDA		REFP_ADC	AC5	PP1V25_SLPS2R_SMC_AVREF		45
						REFM_ADC	AC4	GND_SMC_AVSS		PLACE_NEAR=U3900.AC4:4MM
48	OUT	I2C_DISP_SCL	L2	SMC_I2C3_SCL						
48	BI	I2C_DISP_SDA	P5	SMC_I2C3_SDA		SMC_PWM0	E2	SMC_FAN_0_PWM	OUT	57
						SMC_TACH0	K6	SMC_FAN_0_TACH	IN	57
106 48	OUT	I2C_PWR_SCL	L1	SMC_I2C4_SCL						
106 48	BI	I2C_PWR_SDA	M1	SMC_I2C4_SDA		SMC_PWM1	N5	NC_SMC_FAN_1_PWM	OUT	46
						SMC_TACH1	L6	NC_SMC_FAN_1_TACH	IN	46
48	OUT	NC_I2C_IOSNS_SCL	N1	SMC_I2C5_SCL						
48	BI	NC_I2C_IOSNS_SDA	N2	SMC_I2C5_SDA		SMC_PWM2	K5	SMC_LED_ONEWIRE	BI	46
108 48	OUT	I2C_SSD_SCL	P1	SMC_I2C6_SCL		(IPU) SMC_UART0_RXD	U2	SMC_DEBUGPRT_RX	IN	95 113
108 48	BI	I2C_SSD_SDA	P4	SMC_I2C6_SDA		SMC_UART0_TXD	T1	SMC_DEBUGPRT_TX	OUT	95 113
						SWD_OUT0_TCK	AB4	SSD0_SWCLK_UART_R2D	OUT	74 75 76 77 78 108
						SWD_OUT0_TMS	Y1	SSD0_SWDIO_UART_D2R	BI	74 75 76 77 78 108
						SWD_OUT1_TCK	AD1	NC_SSD1_SWCLK_UART_R2D	OUT	46
						SWD_OUT1_TMS	W7	NC_SSD1_SWDIO_UART_D2R	BI	46

XW4089
SM
1 2

PP1V8_S5 — 12 16 17 103

R4046	10K	1 2 5% 1/20W MF 201	SOC_JTAG_SEL	38 108
R4047	100K	1 2 5% 1/20W MF 201	SOC_DOCK_CONNECT	29 30 38 106
R4054	100K	1 2 5% 1/20W MF 201	ESPI_IO<0>	12 38 109 113
R4055	100K	1 2 5% 1/20W MF 201	ESPI_IO<1>	12 38 109 113
R4056	100K	1 2 5% 1/20W MF 201	ESPI_IO<2>	12 38 109 113
R4057	100K	1 2 5% 1/20W MF 201	ESPI_IO<3>	12 38 109 113
R4059	100K	1 2 5% 1/20W MF 201	ESPI_CS_L	12 38 113

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE
SoC AOP/AON/SMC

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DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
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OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 4 OF 17

46 IN	GND	B24	MIPI0C_DATA0_P		
46 IN	GND	A24	MIPI0C_DATA0_N		
46 IN	GND	B22	MIPI0C_DATA1_P		
46 IN	GND	A22	MIPI0C_DATA1_N		
46 IN	GND	B23	MIPI0C_CLK_P		
46 IN	GND	A23	MIPI0C_CLK_N		
46 IN	GND	B25	MIPI1C_DATA0_P		
46 IN	GND	A25	MIPI1C_DATA0_N		
46 IN	GND	B27	MIPI1C_DATA1_P		
46 IN	GND	A27	MIPI1C_DATA1_N		
46 IN	GND	B26	MIPI1C_CLK_P		
46 IN	GND	A26	MIPI1C_CLK_N		
46 OUT	GND	B30	MIPID_DATA0_P		
46 OUT	GND	A30	MIPID_DATA0_N		
46 OUT	GND	B29	MIPID_CLK_P		
46 OUT	GND	A29	MIPID_CLK_N		
	SOC_MIPI0C_REXT	F23	MIPI0C_REXT		
	SOC_MIPI1C_REXT	F25	MIPI1C_REXT		
	SOC_MIPID_REXT	F26	MIPID_REXT		
		AC28	ISP_I2C0_SDA	BI 49	NC_I2C_FTCAM_SDA
		AD33	ISP_I2C0_SCL	OUT 49	NC_I2C_FTCAM_SCL
		AA29	ISP_I2C1_SDA	BI 49	NC_I2C_PLCAM_SDA
		AD30	ISP_I2C1_SCL	OUT 49	NC_I2C_PLCAM_SCL
		AF32	SENSOR0_CLK	OUT 46	NC_FTCAM_CLK12M_R
		AF30	SENSOR0_RST	OUT 46	NC_FTCAM_RESET_L
		AC29	SENSOR0_ISTRB	OUT 46	NC_DFR_TOUCH_RESET_L
		AA28	SENSOR1_CLK	OUT 46	NC_PLCAM_RX_CLK12M_R
		AB30	SENSOR1_RST	OUT 46	NC_PLCAM_RX_RESET_L
		AA30	SENSOR1_ISTRB	OUT 46	NC_DFR_DISP_RESET_L
		AB28	SENSOR2_CLK	OUT 46	NC_PLCAM_TX_CLK12M_R
		AD28	SENSOR2_RST	OUT 46	NC_PLCAM_TX_RESET_L
		W28	(IPD) SENSOR_INT	IN 46	NC_PLCAM_TX_INT
		D33	(IPD) DISP_TE	IN 46	NC_DFR_DISP_TE
		L30	DISP_VSYNC	IN 45	BOARD_REV2
		AF29	CLK32K_OUT	OUT 46	NC_DFR_TOUCH_CLK32K_RESET_L

R4100 4.02K 1% 1/20W MF 201
R4101 4.02K 1% 1/20W MF 201
R4102 4.02K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
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49 BI	I2C_SPKRAMP_SDA	W33	I2C0_SDA		
49 OUT	I2C_SPKRAMP_SCL	U30	I2C0_SCL		
49 BI	NC_I2C_SPKRAMP_R_SDA	AB32	I2C1_SDA		
49 OUT	NC_I2C_SPKRAMP_R_SCL	V30	I2C1_SCL		
49 BI	I2C_CODEC_SDA	H30	I2C2_SDA		
49 OUT	I2C_CODEC_SCL	P28	I2C2_SCL		
49 BI	NC_I2C_ALS_SDA	V28	I2C3_SDA		
49 OUT	NC_I2C_ALS_SCL	AB33	I2C3_SCL		
49 BI	NC_I2C_DFR_SDA	L33	I2C4_SDA		
49 OUT	NC_I2C_DFR_SCL	R29	I2C4_SCL		
49 BI	NC_I2C_SOC_5_SDA	M29	I2C5_SDA		
49 OUT	NC_I2C_SOC_5_SCL	R30	I2C5_SCL		
46 IN	NC_SPKR_ID1	J33	I2C6_SDA	(IPU)	
46 IN	NC_SPKR_ID0	L29	I2C6_SCL	(IPU)	
113 IN	SOC_DEBUGPRT_RX	V32	UART0_RXD	(IPU)	
113 OUT	SOC_DEBUGPRT_TX	U32	UART0_TXD		
46 IN	NC_UART_SE_D2R	B15	UART1_RXD		
46 OUT	NC_UART_SE_R2D	A15	UART1_TXD		
46 IN	NC_UART_SE_D2R_CTS_L	D13	UART1_CTS*		
46 OUT	NC_UART_SE_R2D_RTS_L	E12	UART1_RTS*		
34 IN	UART_BT_D2R	F32	UART2_RXD		
34 OUT	UART_BT_R2D	F30	UART2_TXD		
34 IN	UART_BT_D2R_CTS_L	M28	UART2_CTS*		
34 OUT	UART_BT_R2D_RTS_L	K28	UART2_RTS*		
34 IN	UART_BT_LH_D2R	H32	UART3_RXD		
34 OUT	UART_BT_LH_R2D	J32	UART3_TXD		
46 IN	NC_UART_GNSS_D2R_CTS_L	H33	UART3_CTS*		
46 OUT	NC_UART_GNSS_R2D_RTS_L	P30	UART3_RTS*		
36 35 IN	UART_WLAN_D2R	B14	UART4_RXD		
36 35 OUT	UART_WLAN_R2D	A14	UART4_TXD		
36 35 IN	UART_WLAN_D2R_CTS_L	C13	UART4_CTS*		
36 35 OUT	UART_WLAN_R2D_RTS_L	D12	UART4_RTS*		
		AN6	SPI0_MISO	IN 45	SPI_SOCROM_MISO
		AM4	SPI0_MOSI		SPI_SOCROM_MOSI_R
		AN3	SPI0_SCLK		SPI_SOCROM_CLK_R
		AP6	SPI0_SSIN		SPI_SOCROM_CS_L_R
		K30	SPI1_MISO	IN 45	SPI_TPAD_MISO
		J30	SPI1_MOSI	OUT 46	SPI_TPAD_MOSI
		K33	SPI1_SCLK	OUT 46	SPI_TPAD_CLK
		R28	SPI1_SSIN	OUT 46	NC_SPI_TPAD_CS_L
		B17	SPI2_MISO	IN 46	NC_SPI_MESA_MISO
		C17	SPI2_MOSI	OUT 46	NC_SPI_MESA_MOSI_R
		D16	SPI2_SCLK	OUT 46	NC_SPI_MESA_CLK_R
		A17	SPI2_SSIN	OUT 36 108	WLAN_JTAG_TDI
		C14	SPI3_MISO	IN 46	NC_SPI_DFR_MISO
		D15	SPI3_MOSI	OUT 46	NC_SPI_DFR_MOSI_R
		C16	SPI3_SCLK	OUT 46	NC_SPI_DFR_CLK_R
		A16	SPI3_SSIN	OUT 46	NC_SPI_DFR_CS_L
		Y28	(IPD) I2S0_DIN	IN 46	I2S_SPKRAMP_D2R_RR
		AC32	I2S0_DOUT	OUT 46	I2S_SPKRAMP_R2D_R
		Y29	I2S0_BCLK	OUT 46	I2S_SPKRAMP_BCLK_R
		AE32	I2S0_LRCK	OUT 46	I2S_SPKRAMP_LRCLK_R
		AM33	I2S0_MCK	BI 46	NC_DFR_TOUCH_RSVD
		C18	(IPD) I2S1_DIN	IN 46	I2S_SPKRAMP_R_D2R
		E17	I2S1_DOUT	OUT 46	I2S_SPKRAMP_R_R2D_R
		D17	I2S1_BCLK	OUT 46	I2S_SPKRAMP_R_BCLK_R
		B18	I2S1_LRCK	OUT 46	I2S_SPKRAMP_R_LRCLK
		D18	I2S1_MCK	OUT 46	NC_PCHROM_SW_EN
		Y33	(IPD) I2S2_DIN	IN 46	I2S_CODEC_D2R_RR
		AA33	I2S2_DOUT	OUT 46	I2S_CODEC_R2D_R
		AE33	I2S2_BCLK	OUT 46	I2S_CODEC_BCLK_R
		V29	I2S2_LRCK	OUT 46	I2S_CODEC_LRCLK_R
		AL30	I2S2_MCK	OUT 46	NC_I2S_CODEC_MCLK
		R32	(IPD) I2S3_DIN	IN 46	NC_I2S_HAWKING_D2R
		U33	I2S3_DOUT	OUT 46	NC_I2S_CODEC1_R2D_R
		T33	I2S3_BCLK	OUT 46	NC_I2S_HAWKING_BCLK_R
		U29	I2S3_LRCK	OUT 46	NC_I2S_HAWKING_LRCLK
		V33	I2S3_MCK	OUT 46	NC_I2S_SPKRAMP_MCLK_R

PLACE_NEAR=U3900.AM4:5MM
PLACE_NEAR=U3900.AN3:5MM
PLACE_NEAR=U3900.AP6:5MM

R4171 20 1 2 5% 1/20W MF 201 SPI_SOCROM_MOSI OUT 45
R4172 20 1 2 5% 1/20W MF 201 SPI_SOCROM_CLK OUT 45
R4173 20 1 2 5% 1/20W MF 201 SPI_SOCROM_CS_L OUT 45

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 41 OF 142
SHEET 39 OF 115

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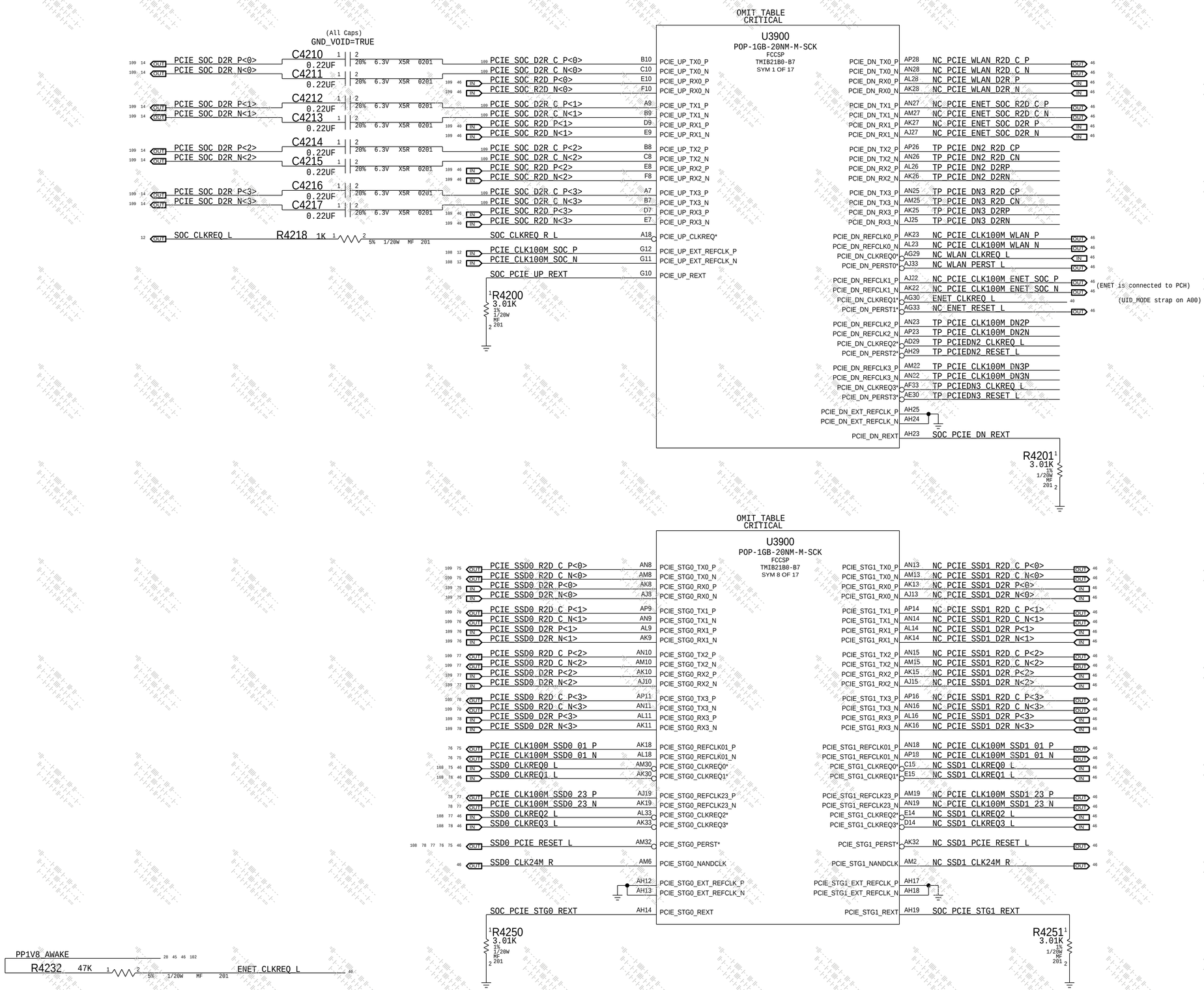

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SoC PCIe

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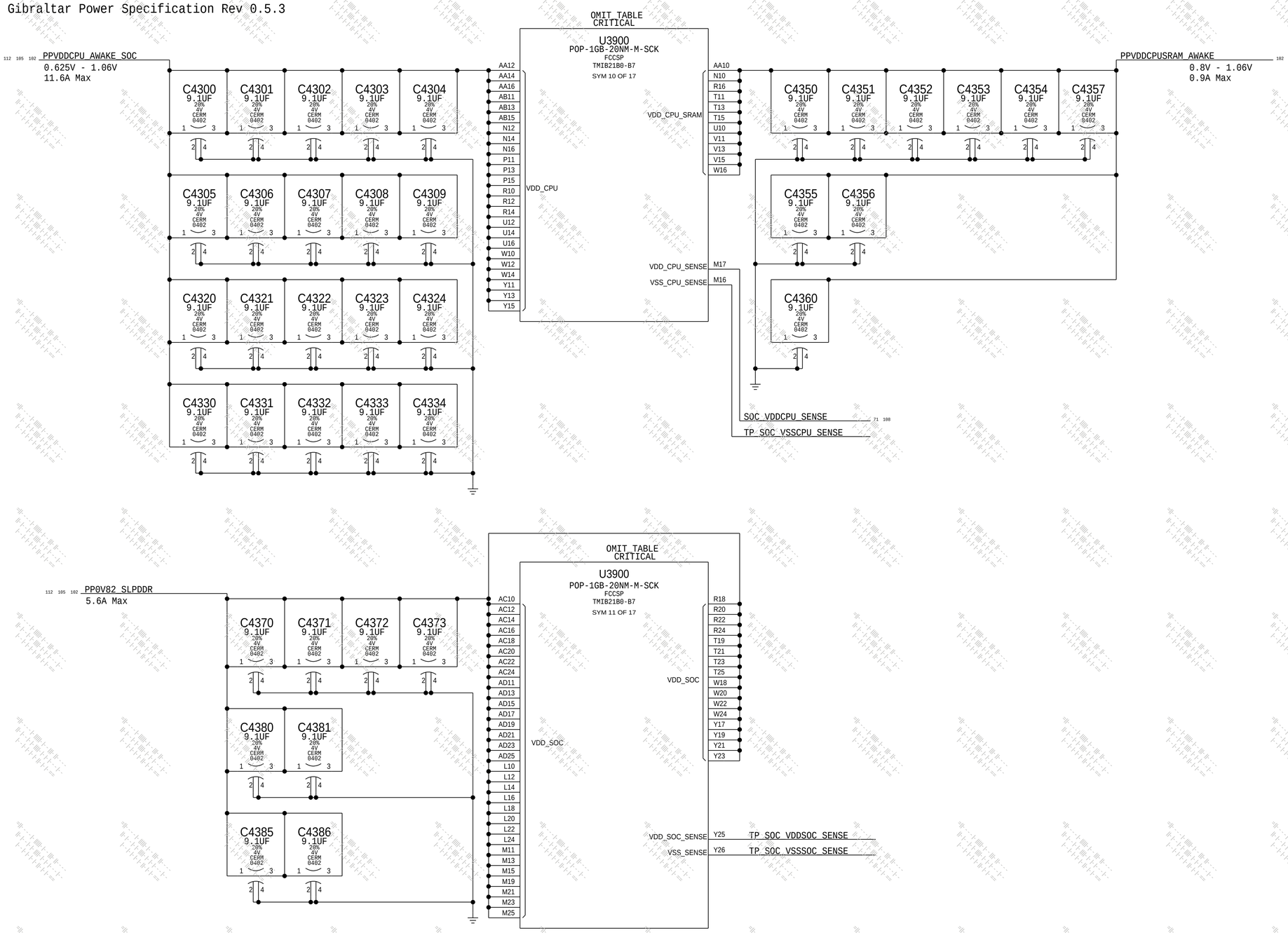
Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC Power 1

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REVISION: 6.0.0

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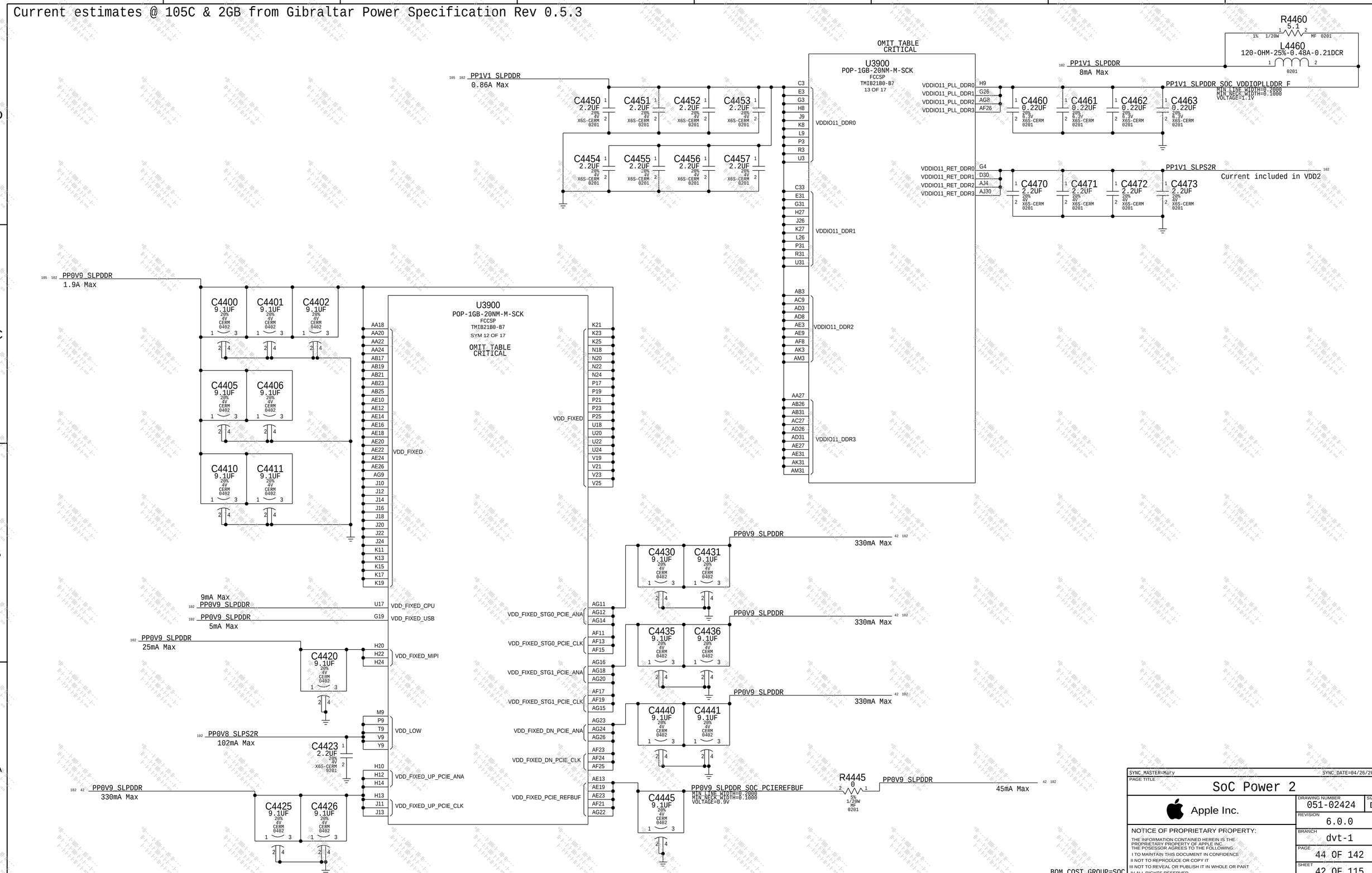
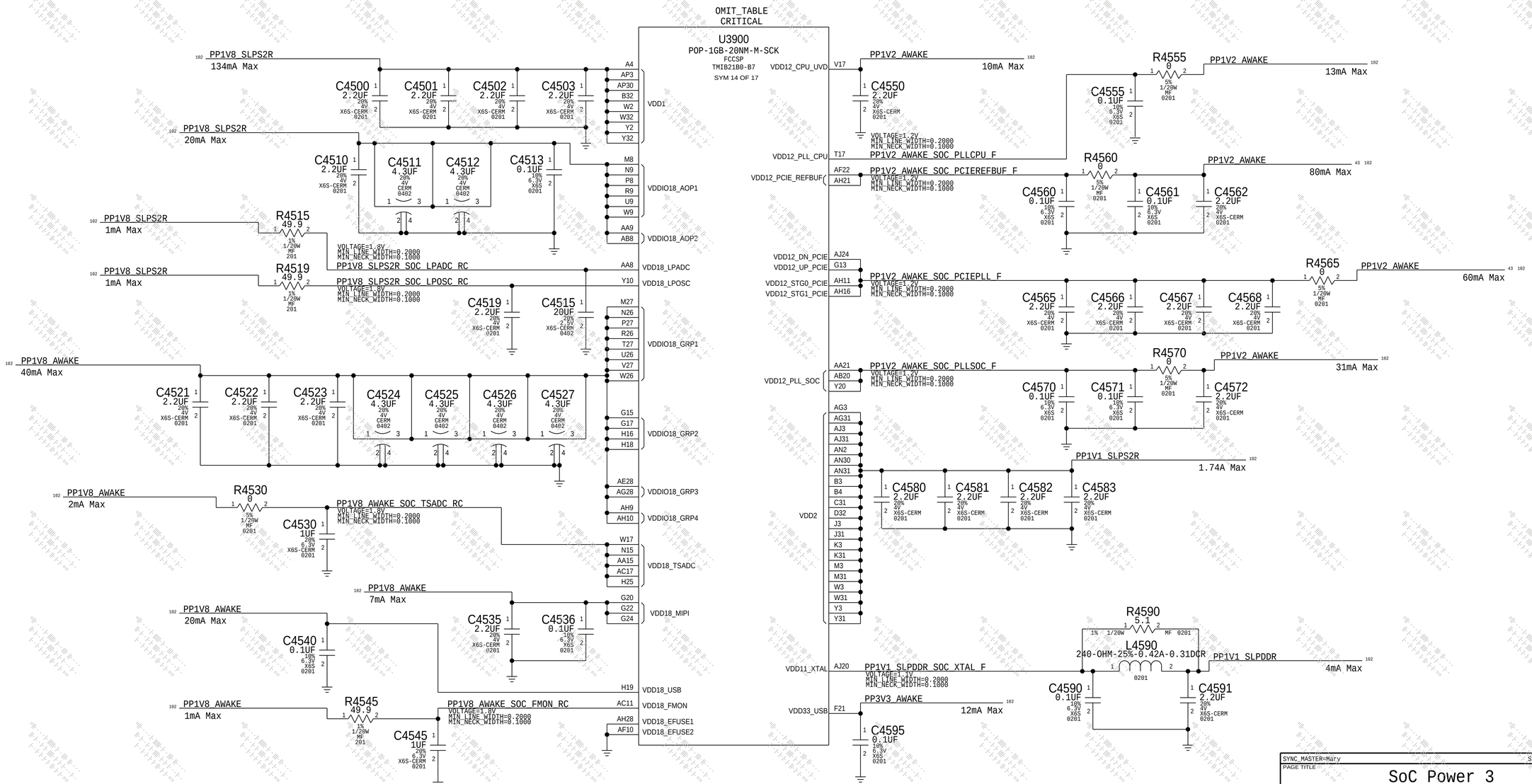


Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC Power 3

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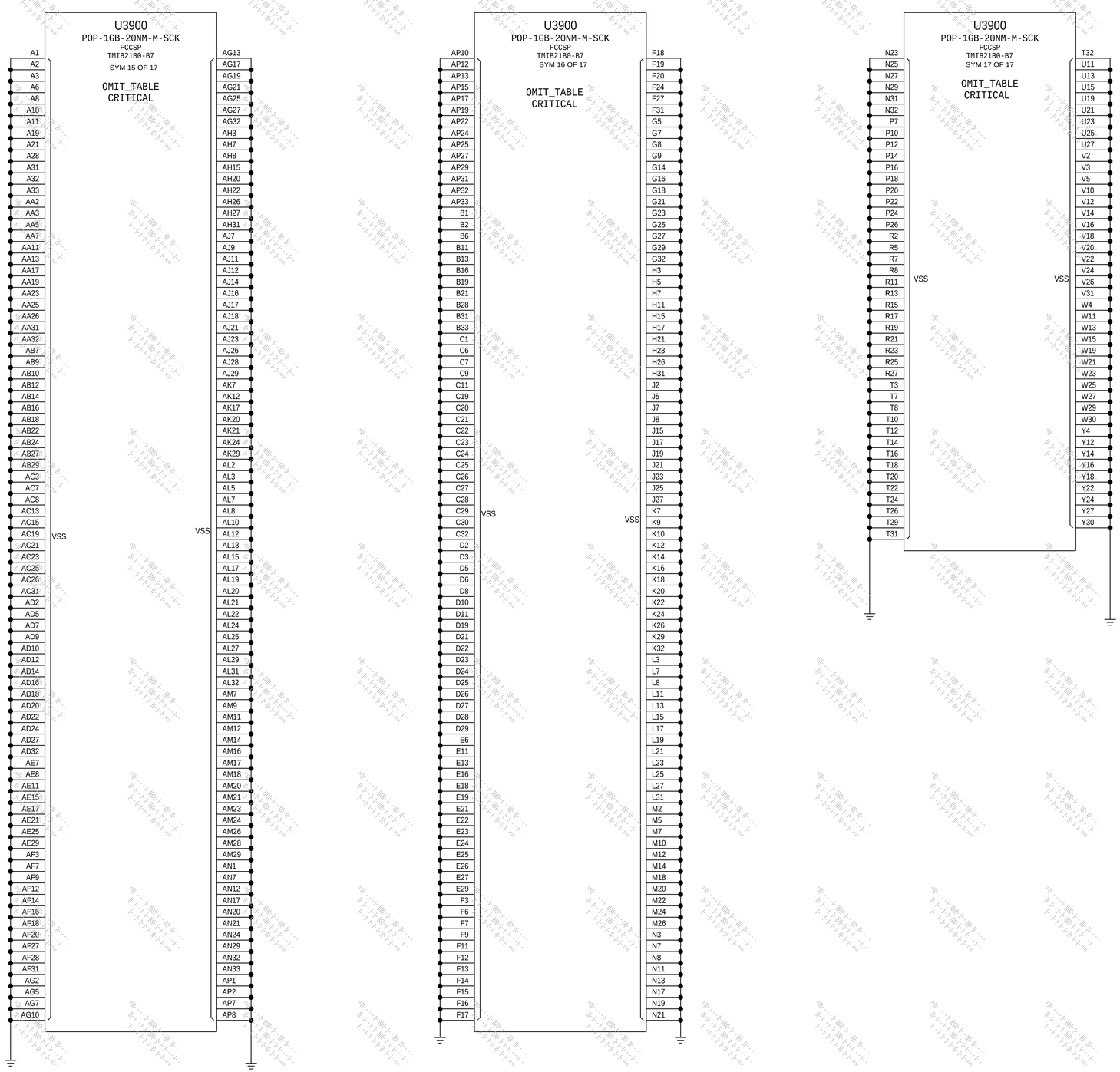

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SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SoC Ground

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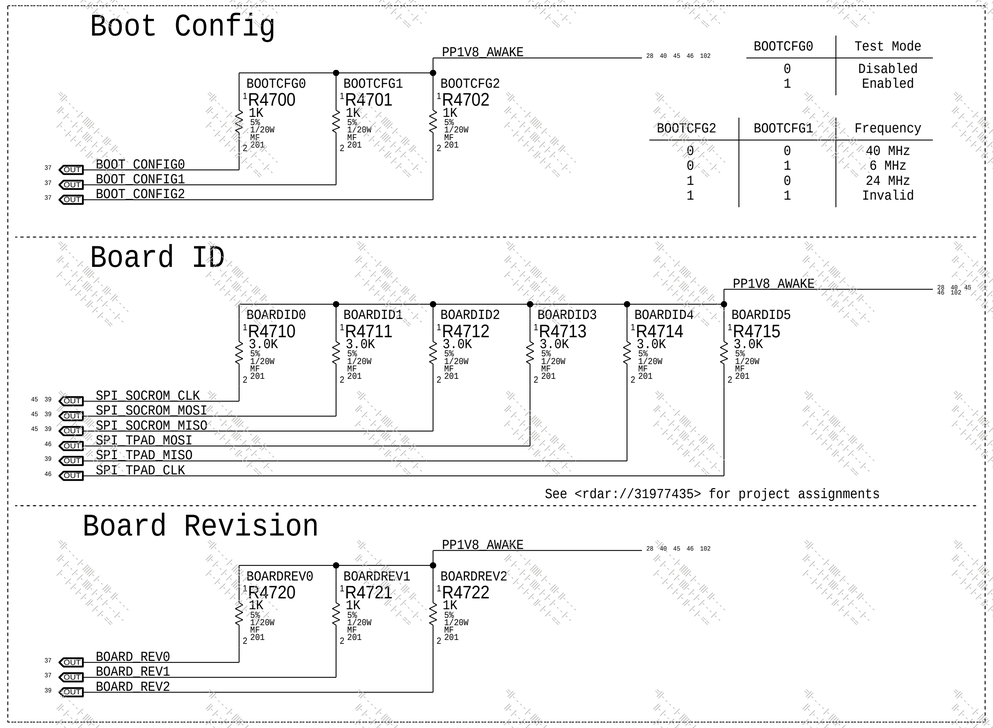
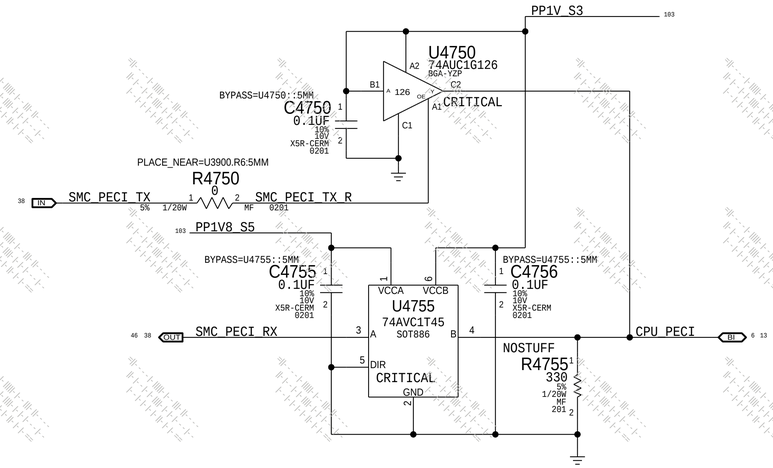


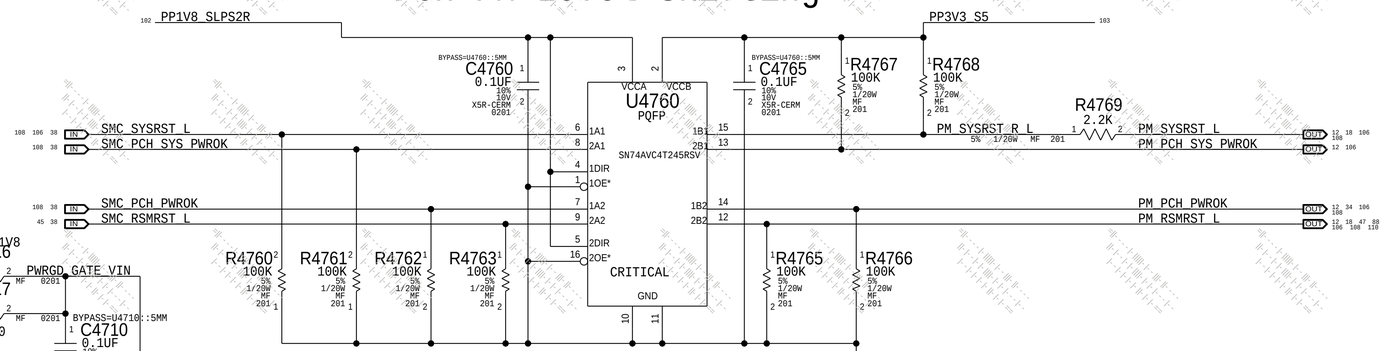
BOOTCFG0	Test Mode
0	Disabled
1	Enabled

BOOTCFG2	BOOTCFG1	Frequency
0	0	40 MHz
0	1	6 MHz
1	0	24 MHz
1	1	Invalid

PECI Level Shifting

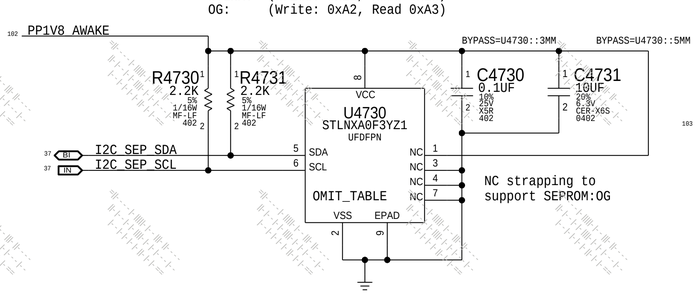


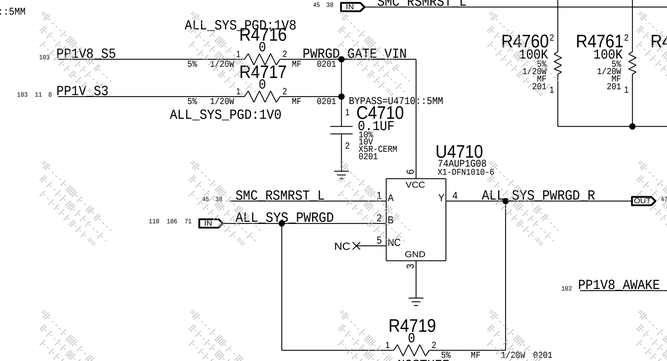
PCH PM Level Shifting



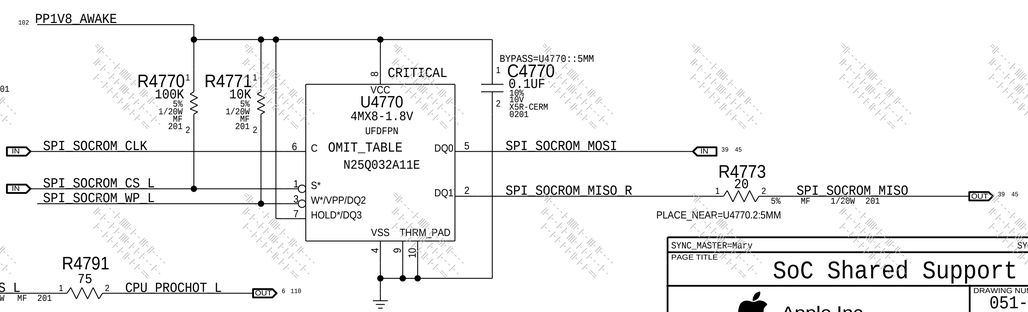
SEP EEPROM

STLNX: (Write: 0xE2, Read 0xE3)
OG: (Write: 0xA2, Read 0xA3)



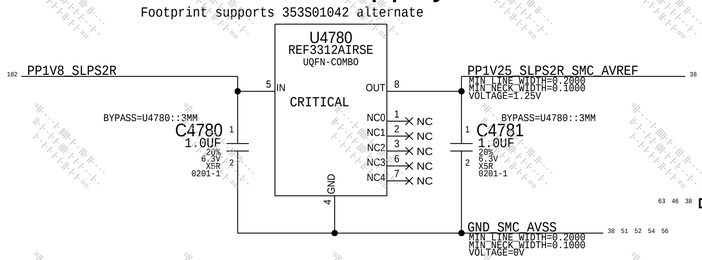


SoC ROM



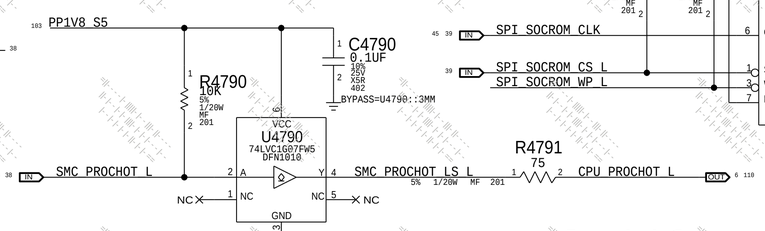
SMC AVREF Supply

Footprint supports 353S01042 alternate



PROCHOT Level Shifter

rdar://problem/36121354



BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC Shared Support

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PCIe Up R2D AC Caps

(All Caps)
GND_VOID=TRUE

PCIE SOC R2D C P<0>	C4820	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D P<0>	109 14	40 109
PCIE SOC R2D C N<0>	C4821	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D N<0>	109 14	40 109
PCIE SOC R2D C P<1>	C4822	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D P<1>	109 14	40 109
PCIE SOC R2D C N<1>	C4823	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D N<1>	109 14	40 109
PCIE SOC R2D C P<2>	C4824	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D P<2>	109 14	40 109
PCIE SOC R2D C N<2>	C4825	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D N<2>	109 14	40 109
PCIE SOC R2D C P<3>	C4826	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D P<3>	109 14	40 109
PCIE SOC R2D C N<3>	C4827	0.22UF	20%	6.3V	X5R	0201	PCIE SOC R2D N<3>	109 14	40 109

GPIO Source Termination

I2S SPKRAMP R2D R	R4843	33	5%	1/20W	MF	201	I2S SPKRAMP R2D	39	60
I2S SPKRAMP BCLK R	R4844	33	5%	1/20W	MF	201	I2S SPKRAMP BCLK	39	60
I2S SPKRAMP_LRCLK_R	R4865	33	5%	1/20W	MF	201	I2S_SPKRAMP_LRCLK	39	60
I2S CODEC R2D R	R4847	33	5%	1/20W	MF	201	I2S CODEC R2D	39	59
I2S CODEC BCLK R	R4848	33	5%	1/20W	MF	201	I2S CODEC BCLK	39	59
I2S CODEC D2R	R4863	33	5%	1/20W	MF	201	I2S CODEC D2R RR	59	39
I2S CODEC_LRCLK R	R4864	33	5%	1/20W	MF	201	I2S CODEC LRCLK	39	59
I2S SPKRAMP D2R	R4852	0	5%	1/20W	MF	0201	I2S SPKRAMP D2R RR	60	39
SPI TPAD MOSI	—						SPI TPAD MOSI (MAKE_BASE=TRUE)	39	45
SPI TPAD CLK	—						SPI TPAD CLK (MAKE_BASE=TRUE)	39	45
SSD0 CLK24M R	R4857	20	5%	1/20W	MF	201	SSD0 CLK24M	40	46 75 77

PLACE_NEAR=U3900.AC32:5MM
PLACE_NEAR=U3900.Y29:5MM
PLACE_NEAR=U3900.AE32:5MM
PLACE_NEAR=U3900.AA33:5MM
PLACE_NEAR=U3900.AE33:5MM
PLACE_NEAR=U3900.Y33:5MM
PLACE_NEAR=U3900.V29:5MM
PLACE_NEAR=U3900.Y28:5MM
PLACE_NEAR=U3900.AM6:5MM

Misc Alias

CODEC INT L	—	CODEC INT L		59 37
CODEC WAKE L	—	CODEC WAKE L	MAKE_BASE=TRUE	59 38
CODEC RESET L	—	CODEC RESET L	MAKE_BASE=TRUE	59 38
DP2HDMI AOP VDD12ON	—	DP2HDMI AOP VDD12ON	MAKE_BASE=TRUE	38 90
SMC LED ONEWIRE	R4858 0 0201 1/20W 5% MF	SYS LED		38 100 107
TP SMC DEBUG	—	TP SMC DEBUG	MAKE_BASE=TRUE	38 108
PSU11VOC_WAKE_L	—	PSU11VOC_WAKE_L	MAKE_BASE=TRUE	38 87
SMC_GFX_THROTTLE_L	—	SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	87
LIDINT_L_UARTHDD_D2R	—	LIDINT_L_UARTHDD_D2R	MAKE_BASE=TRUE	87
PSU P12V EN L	R4859 0 0201 1/20W 5% MF	SPI DP2HDMI HOLD (SPIHOLD:H9M)		38 20 90
SWD SOC SWCLK	R4800 33 5% 1/20W MF 201	DBGMUX SWD SOC CLK		113 100 38 28
SWD SOC SWDIO	R4801 33 5% 1/20W MF 201	DBGMUX SWD SOC IO		113 100 38 28

Rdar://34600168

PP1V8 SLPS2R — 37 100 102
PP1V8 AWAKE — 28 40 45 102

R4883	47K	5%	1/20W	MF	201	SSD0 CLKREQ0 L	40 75 108	
R4884	47K	5%	1/20W	MF	201	SSD0 CLKREQ1 L	40 76 108	
R4887	47K	5%	1/20W	MF	201	SSD0 CLKREQ2 L	40 77 108	
R4888	47K	5%	1/20W	MF	201	SSD0 CLKREQ3 L	40 78 108	
R4885	100K	5%	1/20W	MF	201	SSD0 PCIE RESET L	40 75 76 77 78 108	
R4886	47K	5%	1/20W	MF	201	SSD0 CLK24M	46 75 77	
R4889	100K	5%	1/20W	MF	201	NC PDM DMIC DATA0	38 46	NOSTUFF
R4890	100K	5%	1/20W	MF	201	NC PDM DMIC DATA1	38 46	NOSTUFF
R4895	100K	5%	1/20W	MF	201	SSD PMU RESET L	37 79 106	

R4845	100K	5%	1/20W	MF	201	I2S_SPKRAMP_R R2D_R	39	NOSTUFF
R4846	100K	5%	1/20W	MF	201	I2S_SPKRAMP_R_BCLK_R	39	NOSTUFF
R4866	100K	5%	1/20W	MF	201	I2S_SPKRAMP_R_D2R	39	NOSTUFF
R4867	100K	5%	1/20W	MF	201	I2S_SPKRAMP_R_LRCLK	39	NOSTUFF

SMC (Fast) ADC Assignments

P12VIN_V	51	SMC_P12VIN_VSENSE	SMC_P12VIN_VSENSE	MAKE_BASE=TRUE	38
P12VIN_I		SMC_P12VIN_ISENSE	SMC_P12VIN_ISENSE	MAKE_BASE=TRUE	38
CPU_HS_I		SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	38
CPUCORE_I		SMC_CPU_VCC_ISENSE	SMC_CPU_VCC_ISENSE	MAKE_BASE=TRUE	38
CPUCORE_V	108 56	SMC_CPU_VCC_VSENSE	SMC_CPU_VCC_VSENSE	MAKE_BASE=TRUE	38
CPUGT_V	108 56	SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE	MAKE_BASE=TRUE	38
CPUGT_I		SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE	MAKE_BASE=TRUE	38
1V2_S3_I		SMC_P1V2_ISENSE	SMC_P1V2_ISENSE	MAKE_BASE=TRUE	38

Calpe (Slow) ADC Assignments

PMU_VDD_I		PMU_P3V3_CAPLE_ISENSE	PMU_P3V3_CAPLE_ISENSE	MAKE_BASE=TRUE	71
CPUSA_I	54	PMU_CPUSA_ISENSE	PMU_CPUSA_ISENSE	MAKE_BASE=TRUE	71
DDR2V5_I	52	PMU_DDR2V5_ISENSE	PMU_DDR2V5_ISENSE	MAKE_BASE=TRUE	71
VCCIO_I	54	PMU_VCCIO_ISENSE	PMU_VCCIO_ISENSE	MAKE_BASE=TRUE	71 108
P5V_G3S_HS_I(12V)	51	PMU_P5V_G3S_HI_ISENSE	PMU_P5V_G3S_HI_ISENSE	MAKE_BASE=TRUE	71 108
CPUSA_V	108 56	PMU_CPUSA_VSENSE	PMU_CPUSA_VSENSE	MAKE_BASE=TRUE	71 108
USBC_5V_I	56	PMU_P5V_USBC_ISENSE	PMU_P5V_USBC_ISENSE	MAKE_BASE=TRUE	71 108
USBA_5V_I	56	PMU_P5V_USBA_ISENSE	PMU_P5V_USBA_ISENSE	MAKE_BASE=TRUE	71 108
TBT_3V3_I	54	PMU_P3V3_TBT_ISENSE	PMU_P3V3_TBT_ISENSE	MAKE_BASE=TRUE	71 108
SSD0_3V3_I	53	PMU_P3V3_SSD0_ISENSE	PMU_P3V3_SSD0_ISENSE	MAKE_BASE=TRUE	71 108
SSD0_12V_I	53	PMU_PBUS_SSD0_ISENSE	PMU_PBUS_SSD0_ISENSE	MAKE_BASE=TRUE	71 108
P3V3_G3H_HS_I(12V)	51	PMU_P3V3_G3H_HI_ISENSE	PMU_P3V3_G3H_HI_ISENSE	MAKE_BASE=TRUE	71 108
P3V3_G3S_WLANBT_I	56	PMU_P3V3_WLANBT_ISENSE	PMU_P3V3_WLANBT_ISENSE	MAKE_BASE=TRUE	71 108
P3V3_ENET_I	56	PMU_P3V3_ENET_ISENSE	PMU_P3V3_ENET_ISENSE	MAKE_BASE=TRUE	71 108
P12_ENET_I	56	PMU_P12V_ENET_ISENSE	PMU_P12V_ENET_ISENSE	MAKE_BASE=TRUE	71 108

WLAN connects to PCH

NC PCIE WLAN R2D C P	—	NC PCIE WLAN R2D C P	40
NC PCIE WLAN R2D C N	—	NC PCIE WLAN R2D C N	40
NC PCIE WLAN D2R P	—	NC PCIE WLAN D2R P	40
NC PCIE WLAN D2R N	—	NC PCIE WLAN D2R N	40

ENET connects to PCH

NC PCIE ENET SOC R2D C P	—	NC PCIE ENET SOC R2D C P	40
NC PCIE ENET SOC R2D C N	—	NC PCIE ENET SOC R2D C N	40
NC PCIE ENET SOC D2R P	—	NC PCIE ENET SOC D2R P	40
NC PCIE ENET SOC D2R N	—	NC PCIE ENET SOC D2R N	40

NC SPKR ID1	—	NC SPKR ID1	39
NC SPKR ID0	—	NC SPKR ID0	39
NC SMC FAN 1 PWM	—	NC SMC FAN 1 PWM	38
NC SMC FAN 1 TACH	—	NC SMC FAN 1 TACH	38
NC WLAN PERST L	—	NC WLAN PERST L	38
NC WLAN CLKREQ L	—	NC WLAN CLKREQ L	40
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39
GND	—	GND	39

No MIPI

NC ENET RESET L	—	NC ENET RESET L	40
NC UART GNSS D2R CTS L	—	NC UART GNSS D2R CTS L	39
NC UART GNSS R2D RTS L	—	NC UART GNSS R2D RTS L	39
NC UART SE D2R	—	NC UART SE D2R	39
NC UART SE R2D	—	NC UART SE R2D	39
NC UART SE D2R CTS L	—	NC UART SE D2R CTS L	39
NC UART SE R2D RTS L	—	NC UART SE R2D RTS L	39
NC PCIE CLK100M WLAN P	—	NC PCIE CLK100M WLAN P	40
NC PCIE CLK100M WLAN N	—	NC PCIE CLK100M WLAN N	40
NC PCIE CLK100M ENET SOC P	—	NC PCIE CLK100M ENET SOC P	40
NC PCIE CLK100M ENET SOC N	—	NC PCIE CLK100M ENET SOC N	40
NC PCIE CLK100M SSD1 01 P	—	NC PCIE CLK100M SSD1 01 P	40
NC PCIE CLK100M SSD1 01 N	—	NC PCIE CLK100M SSD1 01 N	40
NC PCIE CLK100M SSD1 23 P	—	NC PCIE CLK100M SSD1 23 P	40
NC PCIE CLK100M SSD1 23 N	—	NC PCIE CLK100M SSD1 23 N	40

(WIFI is connected to PCH)
(ENET is connected to PCH)

No SSD on Port 1

NC SSD1 CLKREQ0 L	—	NC SSD1 CLKREQ0 L	40
NC SSD1 CLKREQ1 L	—	NC SSD1 CLKREQ1 L	40
NC SSD1 CLKREQ2 L	—	NC SSD1 CLKREQ2 L	40
NC SSD1 CLKREQ3 L	—	NC SSD1 CLKREQ3 L	40
NC SSD1 PCIE RESET L	—	NC SSD1 PCIE RESET L	40
NC SSD1 CLK24M R	—	NC SSD1 CLK24M R	40
NC DFR TOUCH RSVD	—	NC DFR TOUCH RSVD	39

SoC NC Pins

	NC PLCAM TX THROTTLE	—	NC PLCAM TX THROTTLE	MAKE_BASE=TRUE
37	NC GNSS HOST TIME	—	NC GNSS HOST TIME	MAKE_BASE=TRUE
37	NC GNSS DEV WAKE	—	NC GNSS DEV WAKE	MAKE_BASE=TRUE
	NC SE CTLR FW DWLD	—	NC SE CTLR FW DWLD	MAKE_BASE=TRUE
	NC MESA INT	—	NC MESA INT	MAKE_BASE=TRUE
37	NC MESA PWR EN	—	NC MESA PWR EN	MAKE_BASE=TRUE
37	NC WLAN DEV WAKE	—	NC WLAN DEV WAKE	MAKE_BASE=TRUE
37	NC TPAD SPI EN	—	NC TPAD SPI EN	MAKE_BASE=TRUE
	NC SE DEV WAKE	—	NC SE DEV WAKE	MAKE_BASE=TRUE
37	NC DFR DISP INT	—	NC DFR DISP INT	MAKE_BASE=TRUE
37	NC DFR PWR EN	—	NC DFR PWR EN	MAKE_BASE=TRUE
	NC SEP CAM DISABLE L	—	NC SEP CAM DISABLE L	MAKE_BASE=TRUE
	NC SEP DMIC DISABLE L	—	NC SEP DMIC DISABLE L	MAKE_BASE=TRUE
37	NC SEP DISABLE STROBE	—	NC SEP DISABLE STROBE	MAKE_BASE=TRUE
38	NC SPI DESCRIPTOR OVERRIDE L	—	NC SPI DESCRIPTOR OVERRIDE L	MAKE_BASE=TRUE
38	NC GYRO INT1	—	NC GYRO INT1	MAKE_BASE=TRUE
38	NC GYRO INT2	—	NC GYRO INT2	MAKE_BASE=TRUE
38	NC SPI GYRO CS L	—	NC SPI GYRO CS L	MAKE_BASE=TRUE
	NC ALTIMETER INT	—	NC ALTIMETER INT	MAKE_BASE=TRUE
38	NC SPI ALTIMETER CS L	—	NC SPI ALTIMETER CS L	MAKE_BASE=TRUE
39	NC I2S CODEC MCLK	—	NC I2S CODEC MCLK	MAKE_BASE=TRUE
38	NC PDM DMIC CLK0 R	—	NC PDM DMIC CLK0 R	MAKE_BASE=TRUE
38	NC PDM DMIC CLK1 R	—	NC PDM DMIC CLK1 R	MAKE_BASE=TRUE
38	NC PLCAM PROX INT L	—	NC PLCAM PROX INT L	MAKE_BASE=TRUE
38	NC PLCAM ROMEO B2B DETECT	—	NC PLCAM ROMEO B2B DETECT	MAKE_BASE=TRUE
38	NC DFR TOUCH INT L	—	NC DFR TOUCH INT L	MAKE_BASE=TRUE
38	NC SMC GFX SELF THROTTLE	—	NC SMC GFX SELF THROTTLE	MAKE_BASE=TRUE
46 38	NC PDM DMIC DATA0	—	NC PDM DMIC DATA0	MAKE_BASE=TRUE
46 38	NC PDM DMIC DATA1	—	NC PDM DMIC DATA1	MAKE_BASE=TRUE
	NC SMC TOPBLK SWP L	—	NC SMC TOPBLK SWP L	MAKE_BASE=TRUE
38	NC SPI AOP SENSOR MOSI R	—	NC SPI AOP SENSOR MOSI R	MAKE_BASE=TRUE
	NC SPI AOP SENSOR CLK R	—	NC SPI AOP SENSOR CLK R	MAKE_BASE=TRUE
38	NC SPI AOP SENSOR MISO	—	NC SPI AOP SENSOR MISO	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C P<0>	—	NC PCIE SSD1 R2D C P<0>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C N<0>	—	NC PCIE SSD1 R2D C N<0>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C P<1>	—	NC PCIE SSD1 R2D C P<1>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C N<1>	—	NC PCIE SSD1 R2D C N<1>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C P<2>	—	NC PCIE SSD1 R2D C P<2>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C N<2>	—	NC PCIE SSD1 R2D C N<2>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C P<3>	—	NC PCIE SSD1 R2D C P<3>	MAKE_BASE=TRUE
40	NC PCIE SSD1 R2D C N<3>	—	NC PCIE SSD1 R2D C N<3>	MAKE_BASE=TRUE
40	NC PCIE SSD1 D2R P<0>	—	NC PCIE SSD1 D2R P<0>	MAKE_BASE=TRUE
40	NC PCIE SSD1 D2R N<0>	—	NC PCIE SSD1 D2R N<0>	MAKE_BASE=TRUE
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40	NC PCIE SSD1 D2R P<2>	—	NC PCIE SSD1 D2R P<2>	MAKE_BASE=TRUE
40	NC PCIE SSD1 D2R N<2>	—	NC PCIE SSD1 D2R N<2>	MAKE_BASE=TRUE
40	NC PCIE SSD1 D2R P<3>	—	NC PCIE SSD1 D2R P<3>	MAKE_BASE=TRUE
40	NC PCIE SSD1 D2R N<3>	—	NC PCIE SSD1 D2R N<3>	MAKE_BASE=TRUE
38	NC SSD1 SWCLK UART R2D	—	NC SSD1 SWCLK UART R2D	MAKE_BASE=TRUE
38	NC SSD1 SWDIO UART D2R	—	NC SSD1 SWDIO UART D2R	MAKE_BASE=TRUE
39	NC SPI MESA MISO	—	NC SPI MESA MISO	MAKE_BASE=TRUE
39	NC SPI MESA MOSI R	—	NC SPI MESA MOSI R	MAKE_BASE=TRUE
39	NC SPI MESA CLK R	—	NC SPI MESA CLK R	MAKE_BASE=TRUE
39	NC SPI DFR MISO	—	NC SPI DFR MISO	MAKE_BASE=TRUE
39	NC SPI DFR MOSI R	—	NC SPI DFR MOSI R	MAKE_BASE=TRUE
39	NC SPI DFR CLK R	—	NC SPI DFR CLK R	MAKE_BASE=TRUE
39	NC SPI DFR CS L	—	NC SPI DFR CS L	MAKE_BASE=TRUE
38	NC SDCONN STATE CHANGE L	—	NC SDCONN STATE CHANGE L	MAKE_BASE=TRUE
39	NC DFR TOUCH RESET L	—	NC DFR TOUCH RESET L	MAKE_BASE=TRUE
39	NC DFR TOUCH CLK32K RESET L	—	NC DFR TOUCH CLK32K RESET L	MAKE_BASE=TRUE
39	NC DFR DISP TE	—	NC DFR DISP TE	MAKE_BASE=TRUE
39	NC FTCAM CLK12M R	—	NC FTCAM CLK12M R	MAKE_BASE=TRUE
39	NC FTCAM RESET L	—	NC FTCAM RESET L	MAKE_BASE=TRUE
39	NC PLCAM RX CLK12M R	—	NC PLCAM RX CLK12M R	MAKE_BASE=TRUE
39	NC PLCAM RX RESET L	—	NC PLCAM RX RESET L	MAKE_BASE=TRUE
39	NC DFR DISP RESET L	—	NC DFR DISP RESET L	MAKE_BASE=TRUE
39	NC PLCAM TX CLK12M R	—	NC PLCAM TX CLK12M R	MAKE_BASE=TRUE
39	NC PLCAM TX RESET L	—	NC PLCAM TX RESET L	MAKE_BASE=TRUE
39	NC PLCAM TX INT	—	NC PLCAM TX INT	MAKE_BASE=TRUE
39	NC PCHROM SW EN	—	NC PCHROM SW EN	MAKE_BASE=TRUE
38	NC MESA MENUKEY L	—	NC MESA MENUKEY L	MAKE_BASE=TRUE
39	NC I2S HAWKING D2R	—	NC I2S HAWKING D2R	MAKE_BASE=TRUE
39	NC I2S CODEC1 R2D R	—	NC I2S CODEC1 R2D R	MAKE_BASE=TRUE
39	NC I2S HAWKING BCLK R	—	NC I2S HAWKING BCLK R	MAKE_BASE=TRUE
39	NC I2S HAWKING LRCLK	—	NC I2S HAWKING LRCLK	MAKE_BASE=TRUE
39	NC I2S SPKRAMP MCLK R	—	NC I2S SPKRAMP MCLK R	MAKE_BASE=TRUE
39	NC SPI TPAD CS L	—	NC SPI TPAD CS L	MAKE_BASE=TRUE
	NC DISP GCON INT L	—	NC DISP GCON INT L	MAKE_BASE=TRUE

NFC FW downlaod req
T151 Interrupt
NFC/SE device wake
No FaceTime Cam
No Digital Mic
No Altimeter
No GPU
Only for MAF
No Accelerometer
No SSD on Port 1
No GMUX GPIO

63 45 38	SMC_PROCHOT_L	P3MM SM 1	PP	PP4800
45 38	SMC_PECI_RX	P3MM SM 1	PP	PP4801

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SoC Project Support

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 48 OF 142
SHEET: 46 OF 115

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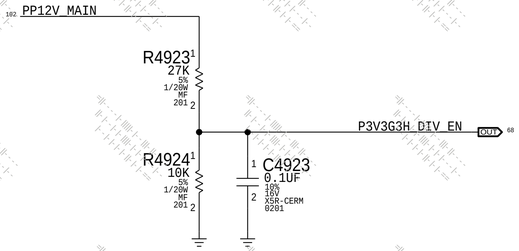
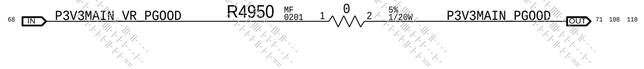
G3H

12V_G3H uses ACDC

3V3_G3H is enabled by PMIC.PVDDMAIN_EN - this is only applied for laptop Big current G3H.
On desktop,3V3_G3H should be enabled by 12V.

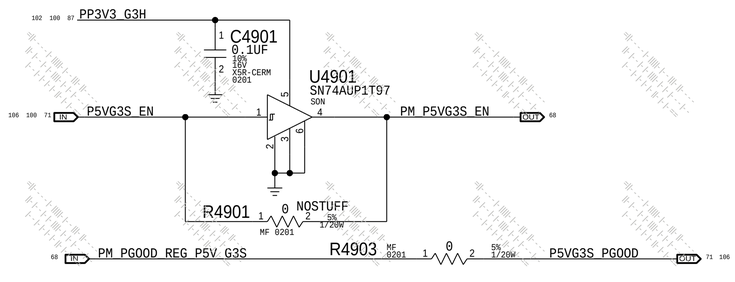


3V3_G3H_PGOOD is to PMIC.GPIO

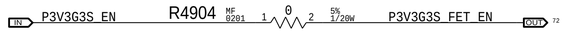


G3S - static timing by PMU

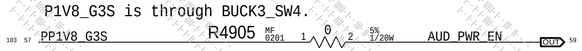
P5V_G3S is enabled by PMIC.GPIO



P3V3_G3S is enabled by PMIC.GPIO



P1V8_G3S is through BUCK3_SW4.



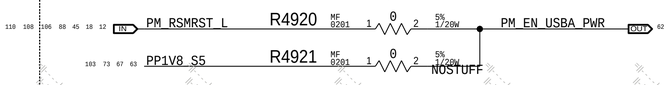
S5 - static timing by PMU

3V3_S5 uses PMU SW

1V8_S5 uses PMU SW

1V05_S5 uses PMU SW

USB-A - HW sequencing

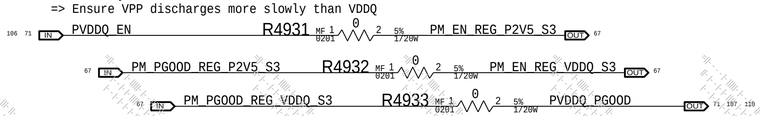


S3

1V2_S3 sequencing

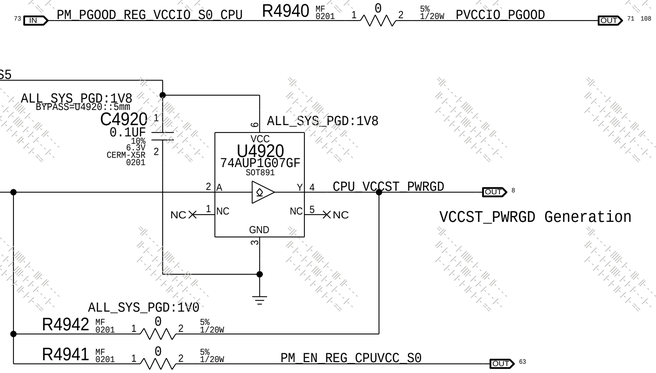
Calpe VDDQ_EN -> 2V5_VTT -> 2V5_PGOOD -> Enable 1V2 VDDQ -> VDDQ_PGDDD

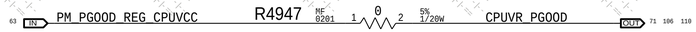
DDR4 Requirement:
VPP > VDDQ at all times
=> Ensure VPP discharges more slowly than VDDQ

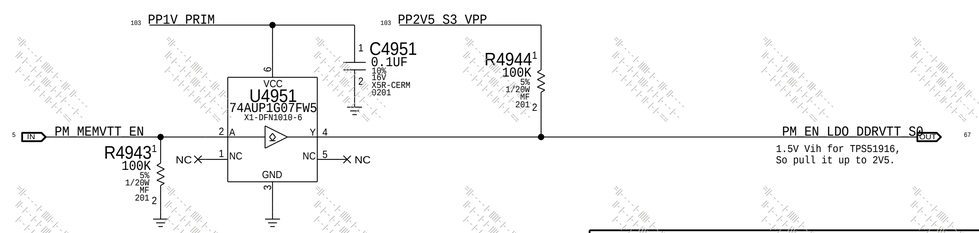


1V05_S3 uses PMU SW

S0 CPU - HW + PMU sequencing







BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-02424 | SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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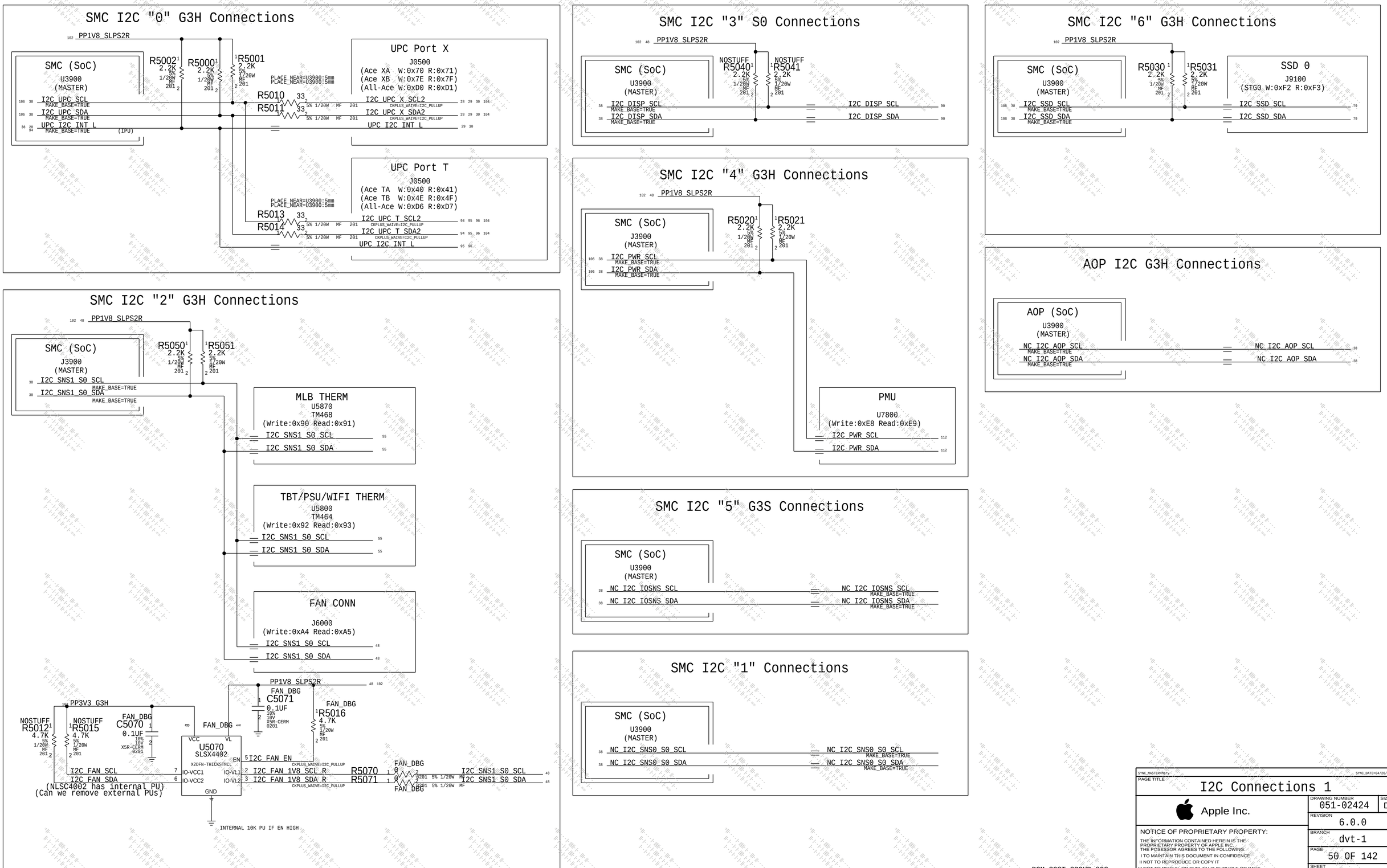
SMC I2C "0" G3H Connections
PP1V8_SLPS2R
SMC (SoC)
U3900
(MASTER)
I2C_UPC_SCL
I2C_UPC_SDA
UPC_I2C_INT_L
MAKE_BASE=TRUE
(IPU)
R5002 2.2K
R5000 2.2K
R5001 2.2K
PLACE_NEAR=U3900:5mm
R5010 33
R5011 33
UPC Port X
J0500
(Ace XA W:0x70 R:0x71)
(Ace XB W:0x7E R:0x7F)
(All-Ace W:0xD0 R:0xD1)
I2C_UPC_X_SCL2
I2C_UPC_X_SDA2
UPC_I2C_INT_L
CKPLUS_WAIVE=I2C_PULLUP
UPC Port T
J0500
(Ace TA W:0x40 R:0x41)
(Ace TB W:0x4E R:0x4F)
(All-Ace W:0xD6 R:0xD7)
R5013 33
R5014 33
I2C_UPC_T_SCL2
I2C_UPC_T_SDA2
SMC I2C "3" S0 Connections
NOSTUFF
R5040 2.2K
R5041 2.2K
I2C_DISP_SCL
I2C_DISP_SDA
SMC I2C "6" G3H Connections
R5030 2.2K
R5031 2.2K
SSD 0
J9100
(STG0 W:0xF2 R:0xF3)
I2C_SSD_SCL
I2C_SSD_SDA
SMC I2C "4" G3H Connections
J3900
R5020 2.2K
R5021 2.2K
I2C_PWR_SCL
I2C_PWR_SDA
PMU
U7800
(Write:0xE8 Read:0xE9)
AOP I2C G3H Connections
AOP (SoC)
NC_I2C_AOP_SCL
NC_I2C_AOP_SDA
SMC I2C "2" G3H Connections
R5050 2.2K
R5051 2.2K
I2C_SNS1_S0_SCL
I2C_SNS1_S0_SDA
MLB THERM
U5870
TM468
(Write:0x90 Read:0x91)
TBT/PSU/WIFI THERM
U5800
TM464
(Write:0x92 Read:0x93)
FAN CONN
J6000
(Write:0xA4 Read:0xA5)
PP3V3_G3H
R5012 4.7K
R5015 4.7K
C5070 0.1UF
C5071 0.1UF
R5016 4.7K
FAN_DBG
U5070
SLSX4402
X2DFN-THICKSTNCL
VCC
VL
EN
IO-VCC1
IO-VCC2
IO-VL1
IO-VL2
GND
I2C_FAN_SCL
I2C_FAN_SDA
I2C_FAN_EN
I2C_FAN_1V8_SCL_R
I2C_FAN_1V8_SDA_R
R5070 0
R5071 0
I2C_SNS1_S0_SCL
I2C_SNS1_S0_SDA
(NLSC4002 has internal PU)
(Can we remove external PUs)
INTERNAL 10K PU IF EN HIGH
SMC I2C "5" G3S Connections
NC_I2C_IOSNS_SCL
NC_I2C_IOSNS_SDA
SMC I2C "1" Connections
NC_I2C_SNS0_S0_SCL
NC_I2C_SNS0_S0_SDA
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
I2C Connections 1
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
PAGE
50 OF 142
SHEET
48 OF 115
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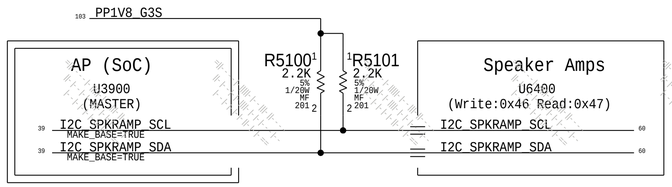
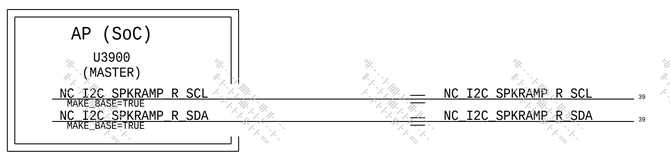
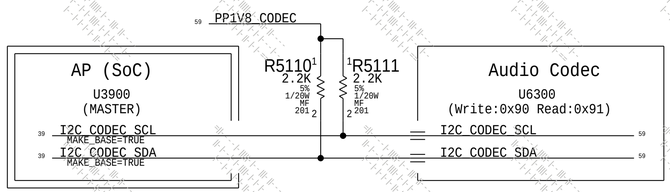
AP I2C "0" G3S Connections



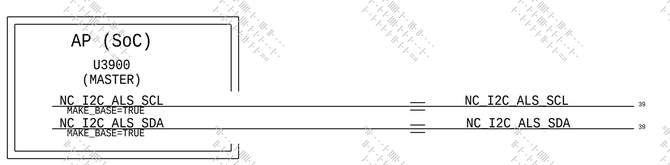
AP I2C "1" G3S Connections



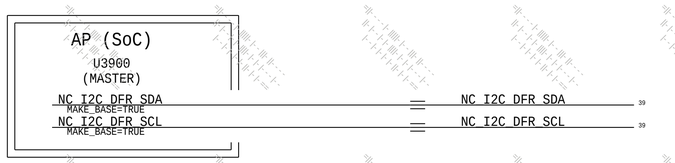
AP I2C "2" Codec Connections



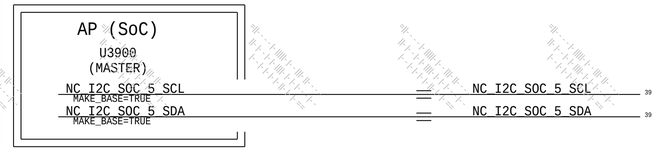
AP I2C "3" S0 Connections



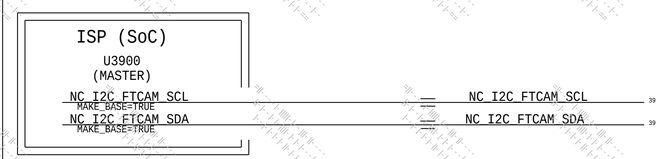
AP I2C "4" HDMI PCON G3S Connections



AP I2C "5" Awake Connections



ISP I2C "0" S0 Connections



ISP I2C "1" G3S Connections

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: I2C Connections 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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SHEET: 49 OF 115

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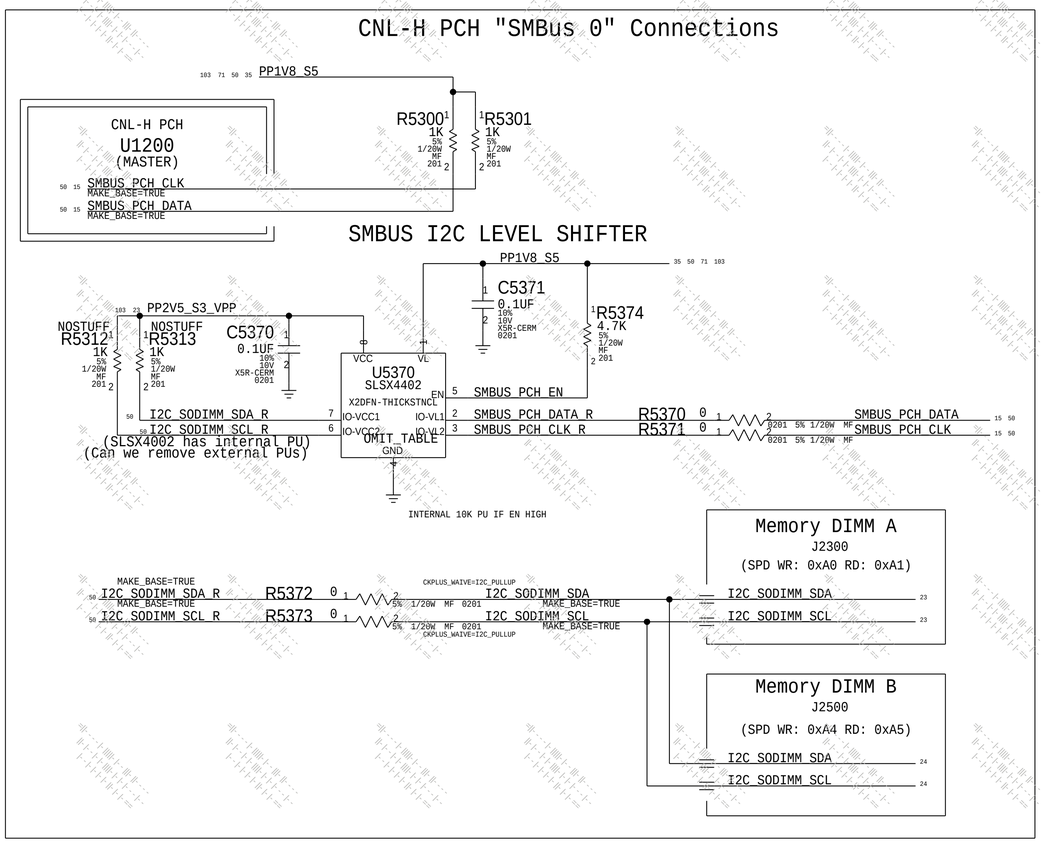

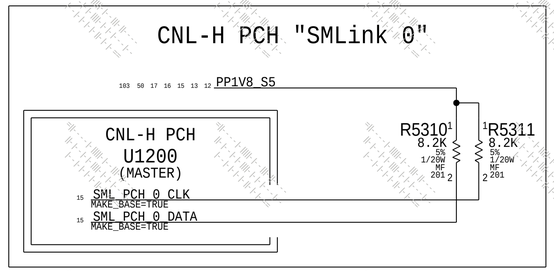

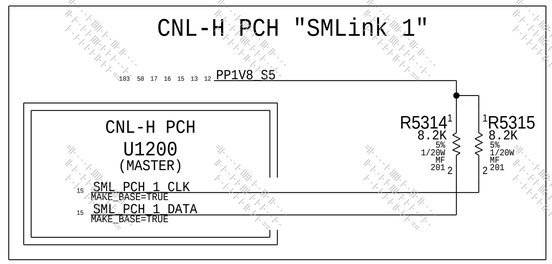

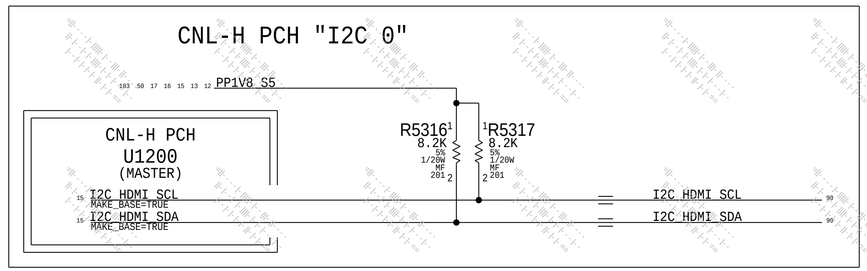

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
311S00179	1	IC,SLSX4402,2BIT D-LVL XLTR,1.8X1.2,DFN8	U5370	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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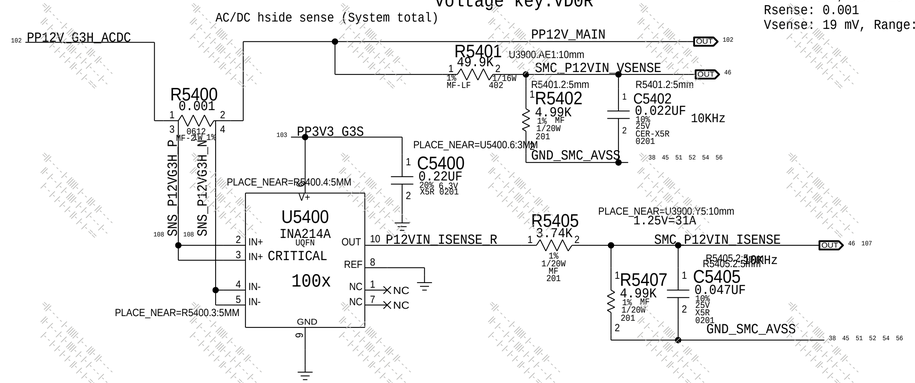
J680 SENSOR SETTINGS

CHIP	Vref(V)	Vmax	SMC sample Freq.	ADR RC filter
H9M	1.25	1.8	10khz	0.1ms
CALPE	1.5	5	10hz	1ms
EADC	2.5	5	1-2hz(10hz)	100ms

PP12V_G3H

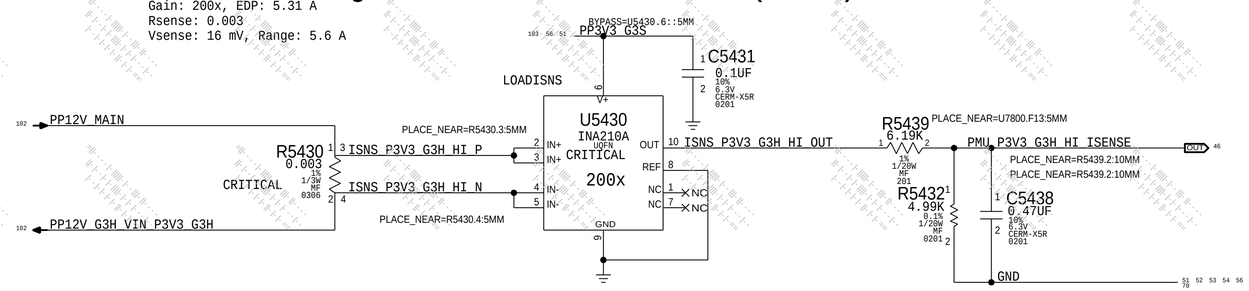
Current key:ID0M
Voltage key:VD0R

Gain: 100x, EDP: 18.75 A
Rsense: 0.001
Vsense: 19 mV, Range: 21.8 A



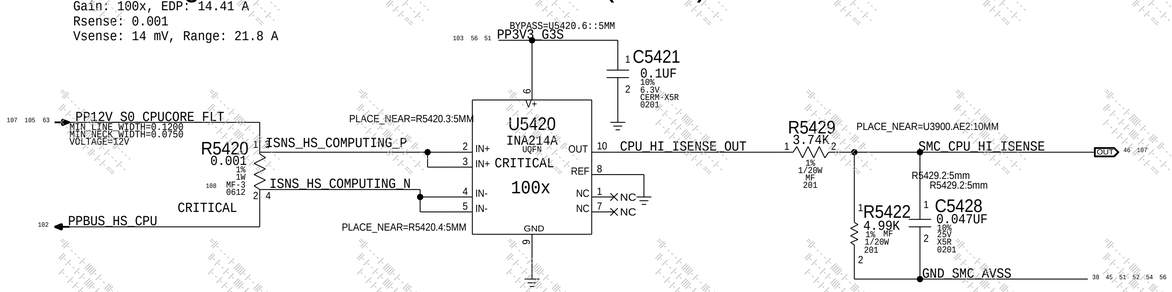
P3V3_G3H High Side Current Sense (IO3R)

Gain: 200x, EDP: 5.31 A
Rsense: 0.003
Vsense: 16 mV, Range: 5.6 A



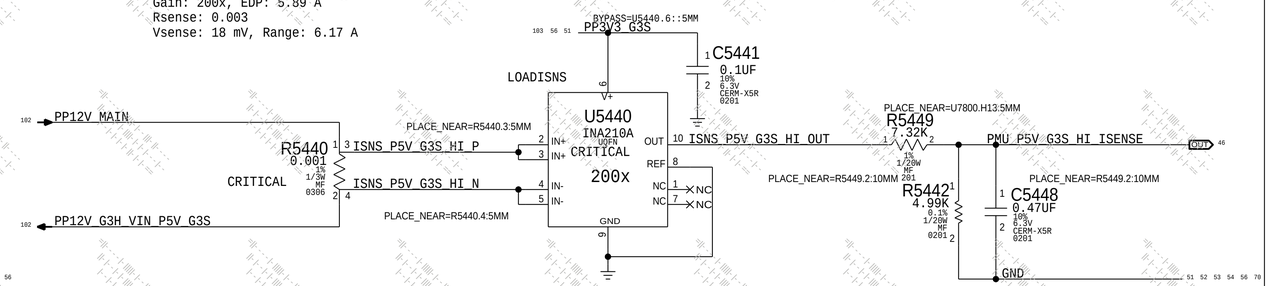
CPU High Side Currrent Sense (IC0R)

Gain: 100x, EDP: 14.41 A
Rsense: 0.001
Vsense: 14 mV, Range: 21.8 A



P5V_G3H High Side Current Sense (IO5R)

Gain: 200x, EDP: 5.89 A
Rsense: 0.003
Vsense: 18 mV, Range: 6.17 A



BOM_COST_GROUP=SENSORS

PAGE TITLE	Power Sensors High Side
	Apple Inc.
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	54 OF 142
SHEET	51 OF 115

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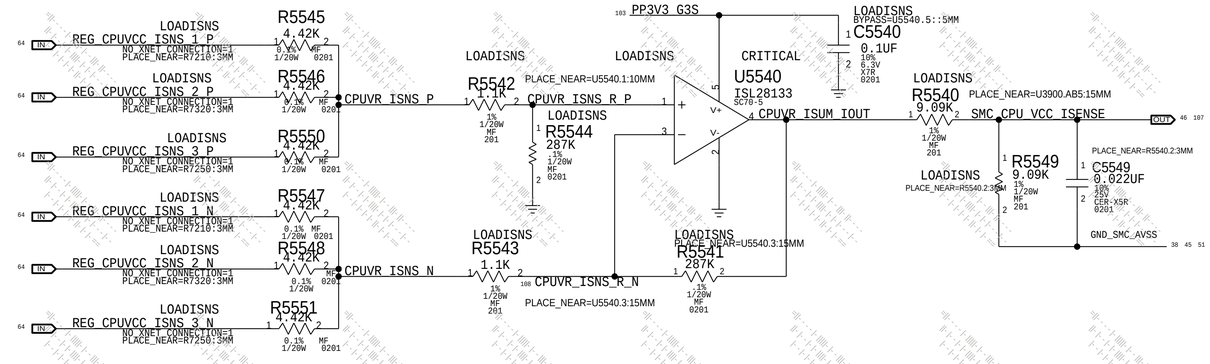
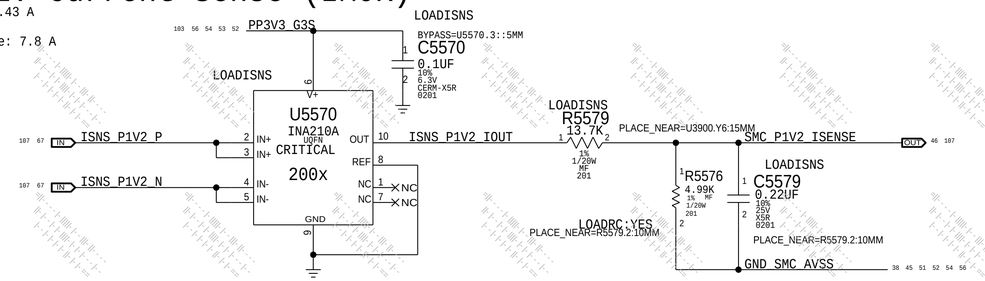
CPU Core Current Sense (ICAC)

Gain: 111.6x, EDP: 128 A
Rsense: 3x of 0.0005
Vsense:22.4 mV, Range: 134.4 A



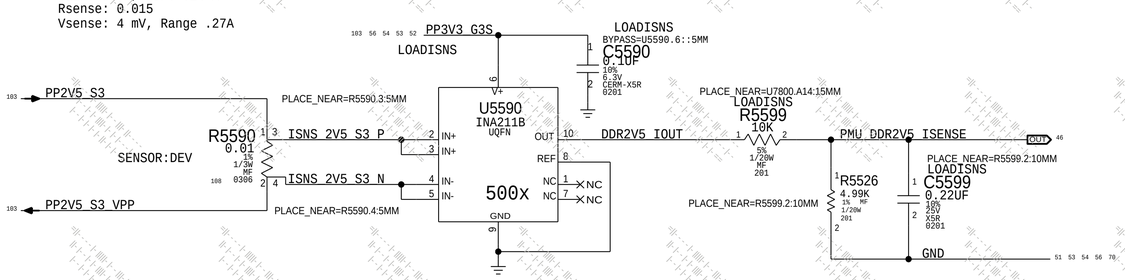
DDR4 1.2V Current Sense (IM0R)

Gain: 200x, EDP: 7.43 A
Rsense: 0.001
Vsense: 7 mV, Range: 7.8 A



2.5V Current Sense (IM0C)

Gain: 500x, EDP: .24 A
Rsense: 0.015
Vsense: 4 mV, Range .27A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5576,R5519,R5549,C5539,R5529		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Load Side

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
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BRANCH: dvt-1
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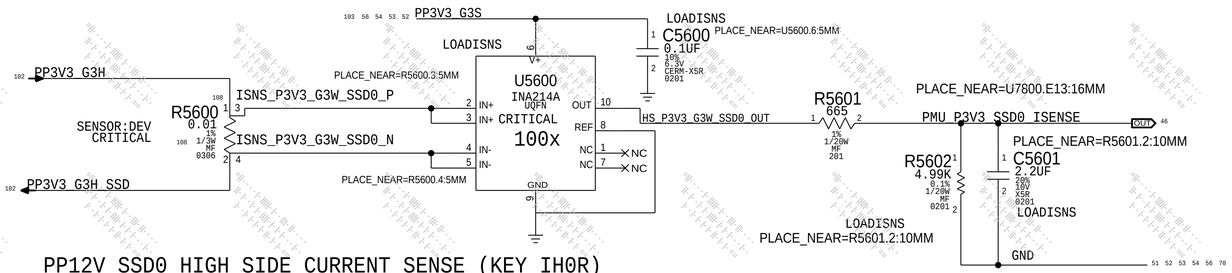
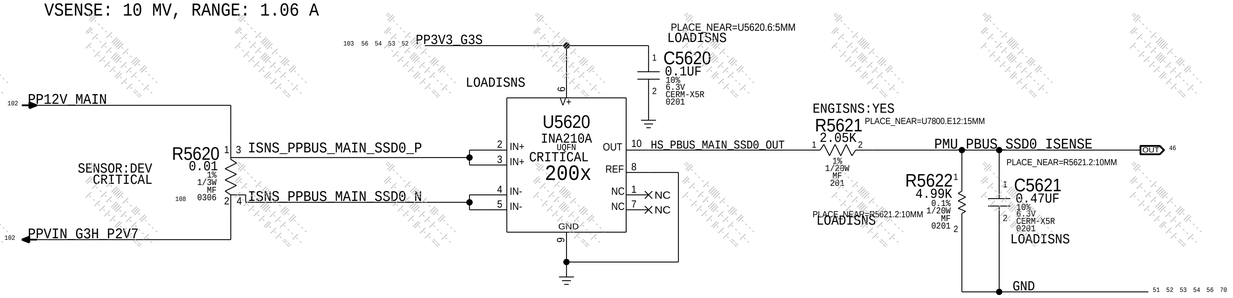
PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (IH0C)

GAIN: 100X, EDP: 1.6 A
RSENSE: 0.01
VSENSE: 16 MV, RANGE: 1.7 A



PP12V_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 1 A
RSENSE: 0.01
VSENSE: 10 MV, RANGE: 1.06 A



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Extended 1

Apple Inc.

DRAWING NUMBER: 051-02424
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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SHEET: 53 OF 115

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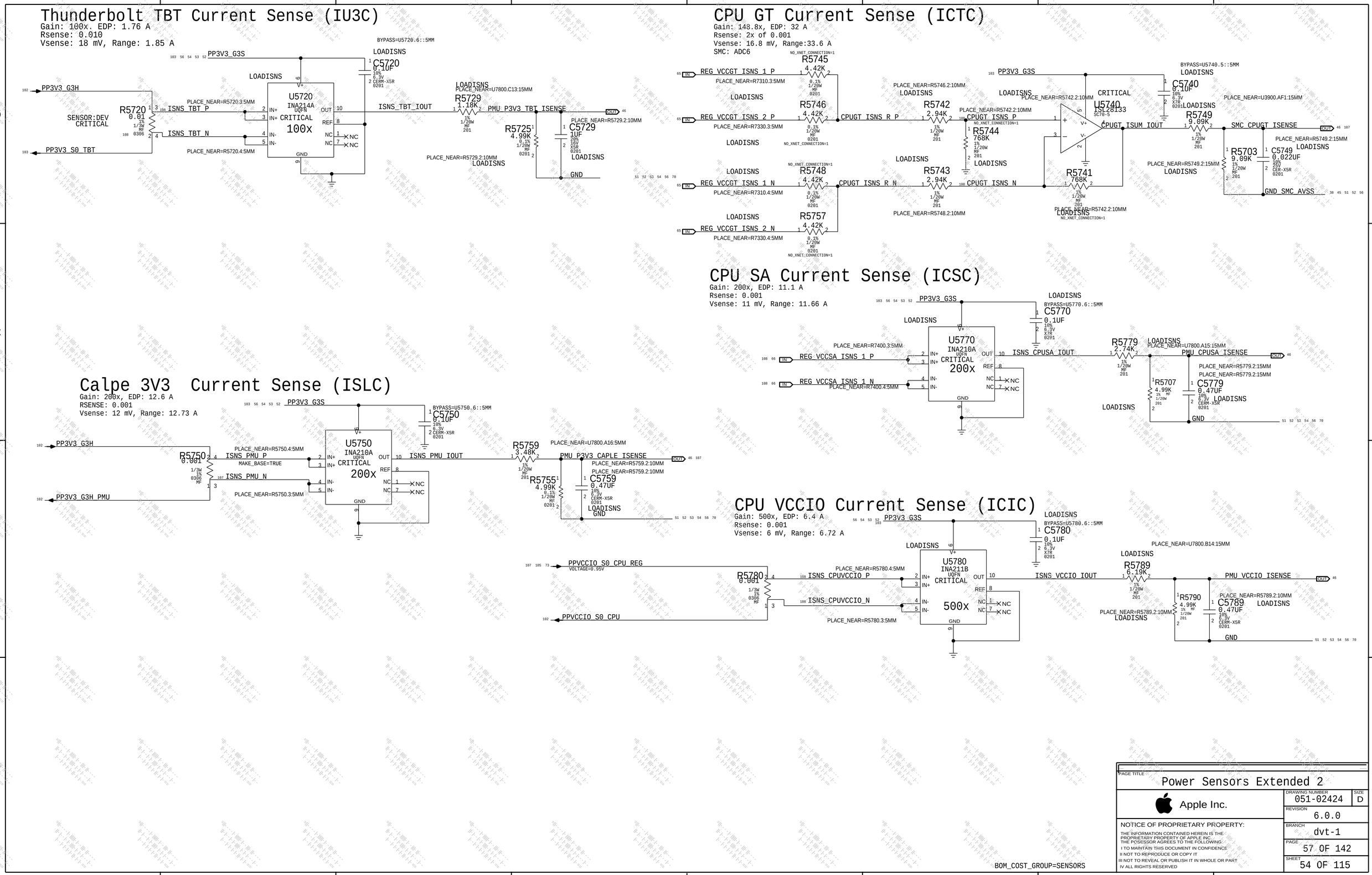

PAGE TITLE
Power Sensors Extended 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 57 OF 142
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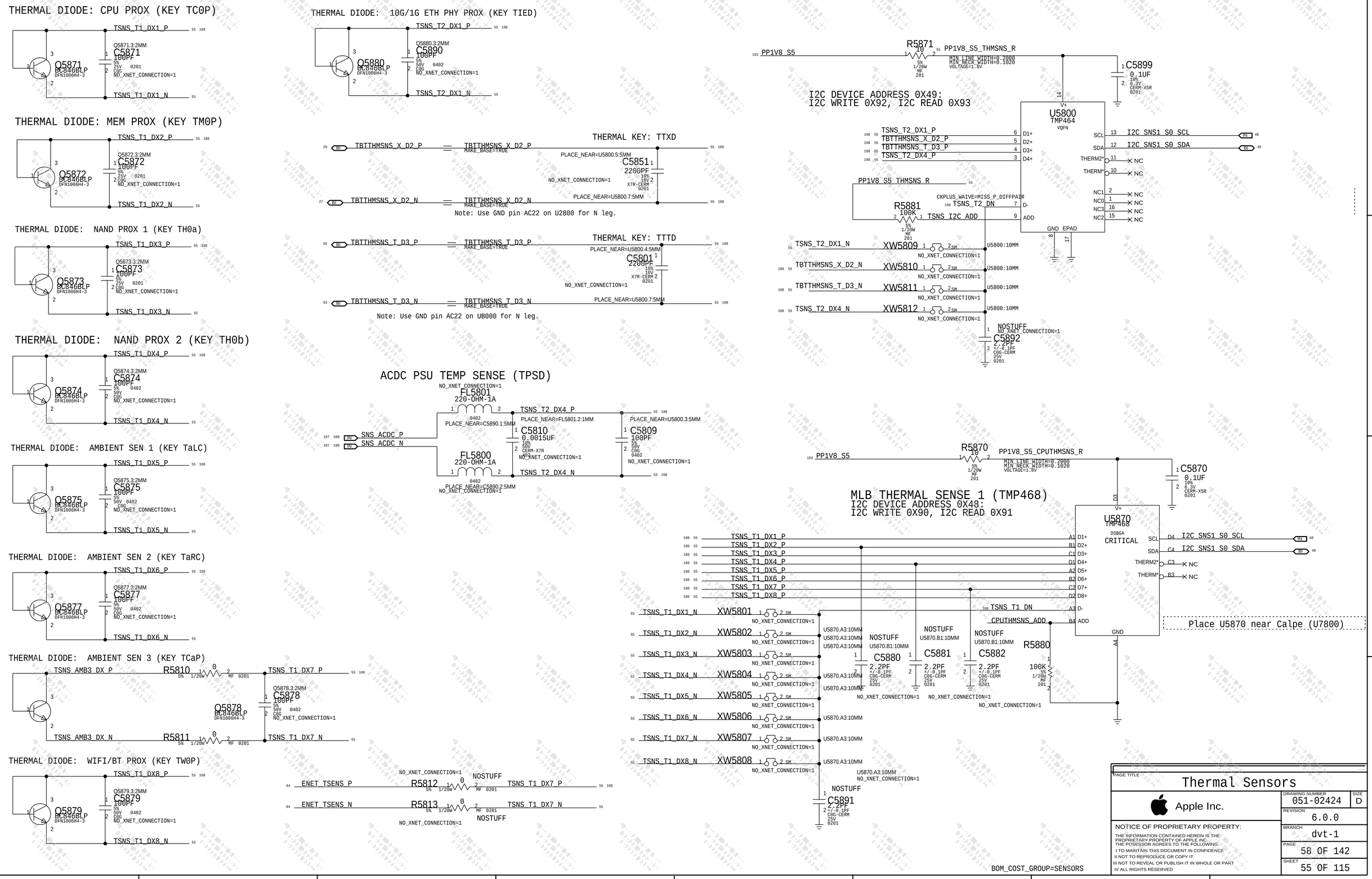
THERMAL DIODE: CPU PROX (KEY TC0P)
TSNS_T1_DX1_P
Q5871 BC846BLP DFN1006H4-3
Q5871:3:2MM C5871 100PF 5% 25V 0201 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX1_N
THERMAL DIODE: 10G/1G ETH PHY PROX (KEY TIED)
TSNS_T2_DX1_P
Q5880 BC846BLP DFN1006H4-3
Q5880:3:2MM C5890 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T2_DX1_N
THERMAL DIODE: MEM PROX (KEY TM0P)
TSNS_T1_DX2_P
Q5872 BC846BLP DFN1006H4-3
Q5872:3:2MM C5872 100PF 5% 25V 0201 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX2_N
THERMAL KEY: TTXD
TBTTHMSNS_X_D2_P
TBTTHMSNS_X_D2_P MAKE_BASE=TRUE
PLACE_NEAR=U5800.5:5MM
C5851 2200PF 10% 10V X7R-CERM 0201
NO_XNET_CONNECTION=1
TBTTHMSNS_X_D2_N
TBTTHMSNS_X_D2_N MAKE_BASE=TRUE
PLACE_NEAR=U5800.7:5MM
Note: Use GND pin AC22 on U2800 for N leg.
THERMAL DIODE: NAND PROX 1 (KEY TH0a)
TSNS_T1_DX3_P
Q5873 BC846BLP DFN1006H4-3
Q5873:3:2MM C5873 100PF 5% 25V 0201 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX3_N
THERMAL KEY: TTTD
TBTTHMSNS_T_D3_P
TBTTHMSNS_T_D3_P MAKE_BASE=TRUE
PLACE_NEAR=U5800.4:5MM
C5801 2200PF 10% 10V X7R-CERM 0201
NO_XNET_CONNECTION=1
TBTTHMSNS_T_D3_N
TBTTHMSNS_T_D3_N MAKE_BASE=TRUE
PLACE_NEAR=U5800.7:5MM
Note: Use GND pin AC22 on UB000 for N leg.
THERMAL DIODE: NAND PROX 2 (KEY TH0b)
TSNS_T1_DX4_P
Q5874 BC846BLP DFN1006H4-3
Q5874:3:2MM C5874 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX4_N
ACDC PSU TEMP SENSE (TPSD)
NO_XNET_CONNECTION=1
FL5801 220-OHM-1A 0402
PLACE_NEAR=C5890.1:5MM
TSNS_T2_DX4_P
PLACE_NEAR=FL5801.2:1MM
C5810 0.0015UF 10% 50V CERM-X7R 0402
NO_XNET_CONNECTION=1
PLACE_NEAR=U5800.3:5MM
C5809 100PF 5% 50V C0G 0402
NO_XNET_CONNECTION=1
SNS_ACDC_P
SNS_ACDC_N
FL5800 220-OHM-1A 0402
PLACE_NEAR=C5890.2:5MM
NO_XNET_CONNECTION=1
TSNS_T2_DX4_N
THERMAL DIODE: AMBIENT SEN 1 (KEY TaLC)
TSNS_T1_DX5_P
Q5875 BC846BLP DFN1006H4-3
Q5875:3:2MM C5875 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX5_N
THERMAL DIODE: AMBIENT SEN 2 (KEY TaRC)
TSNS_T1_DX6_P
Q5877 BC846BLP DFN1006H4-3
Q5877:3:2MM C5877 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX6_N
THERMAL DIODE: AMBIENT SEN 3 (KEY TCaP)
TSNS_AMB3_DX_P
R5810 0 5% 1/20W MF 0201
TSNS_T1_DX7_P
Q5878 BC846BLP DFN1006H4-3
Q5878:3:2MM C5878 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_AMB3_DX_N
R5811 0 5% 1/20W MF 0201
TSNS_T1_DX7_N
THERMAL DIODE: WIFI/BT PROX (KEY TW0P)
TSNS_T1_DX8_P
Q5879 BC846BLP DFN1006H4-3
Q5879:3:2MM C5879 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX8_N
ENET_TSENS_P
R5812 0 5% 1/20W MF 0201 NOSTUFF
ENET_TSENS_N
R5813 0 5% 1/20W MF 0201 NOSTUFF
NO_XNET_CONNECTION=1
PP1V8_S5
R5871 10 5% 1/20W MF 0201
PP1V8_S5_THMSNS_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1020
VOLTAGE=1.8V
C5899 0.1UF 10% 6.3V CERM-X5R 0201
I2C DEVICE ADDRESS 0X49:
I2C WRITE 0X92, I2C READ 0X93
U5800 TMP464 VQFN
TSNS_T2_DX1_P
TBTTHMSNS_X_D2_P
TBTTHMSNS_T_D3_P
TSNS_T2_DX4_P
D1+ D2+ D3+ D4+
SCL SDA
I2C SNS1 S0 SCL
I2C SNS1 S0 SDA
THERM2* THERM*
NC
PP1V8_S5_THMSNS_R
R5881 100K 5% 1/20W MF 201
CKPLUS_WAIVE=MISS_P_DIFFPAIR
TSNS_T2_DN
TSNS_I2C_ADD
D- ADD
NC1 NC0 NC3 NC2
GND_EPAD
TSNS_T2_DX1_N XW5809
TBTTHMSNS_X_D2_N XW5810
TBTTHMSNS_T_D3_N XW5811
TSNS_T2_DX4_N XW5812
SM
NO_XNET_CONNECTION=1
U5800:10MM
NOSTUFF
C5892 2.2PF ±/-0.1PF C0G-CERM 25V 0201
MLB THERMAL SENSE 1 (TMP468)
I2C DEVICE ADDRESS 0X48:
I2C WRITE 0X90, I2C READ 0X91
PP1V8_S5
R5870 10 5% 1/20W MF 201
PP1V8_S5_CPUTHMSNS_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1020
VOLTAGE=1.8V
C5870 0.1UF 10% 6.3V CERM-X5R 0201
U5870 TMP468 DSBGA CRITICAL
TSNS_T1_DX1_P
TSNS_T1_DX2_P
TSNS_T1_DX3_P
TSNS_T1_DX4_P
TSNS_T1_DX5_P
TSNS_T1_DX6_P
TSNS_T1_DX7_P
TSNS_T1_DX8_P
D1+ D2+ D3+ D4+ D5+ D6+ D7+ D8+
SCL SDA
I2C SNS1 S0 SCL
I2C SNS1 S0 SDA
THERM2* THERM*
NC
TSNS_T1_DX1_N XW5801
TSNS_T1_DX2_N XW5802
TSNS_T1_DX3_N XW5803
TSNS_T1_DX4_N XW5804
TSNS_T1_DX5_N XW5805
TSNS_T1_DX6_N XW5806
TSNS_T1_DX7_N XW5807
TSNS_T1_DX8_N XW5808
U5870.A3:10MM
NOSTUFF
C5880 2.2PF ±/-0.1PF C0G-CERM 25V 0201
C5881 2.2PF ±/-0.1PF C0G-CERM 25V 0201
C5882 2.2PF ±/-0.1PF C0G-CERM 25V 0201
U5870.B1:10MM
TSNS_T1_DN
CPUTHMSNS_ADD
R5880 100K 5% 1/20W MF 201
D- ADD
GND
Place U5870 near Calpe (U7800)
C5891 2.2PF ±/-0.1PF C0G-CERM 25V 0201
BOM_COST_GROUP=SENSORS
PAGE TITLE
Thermal Sensors
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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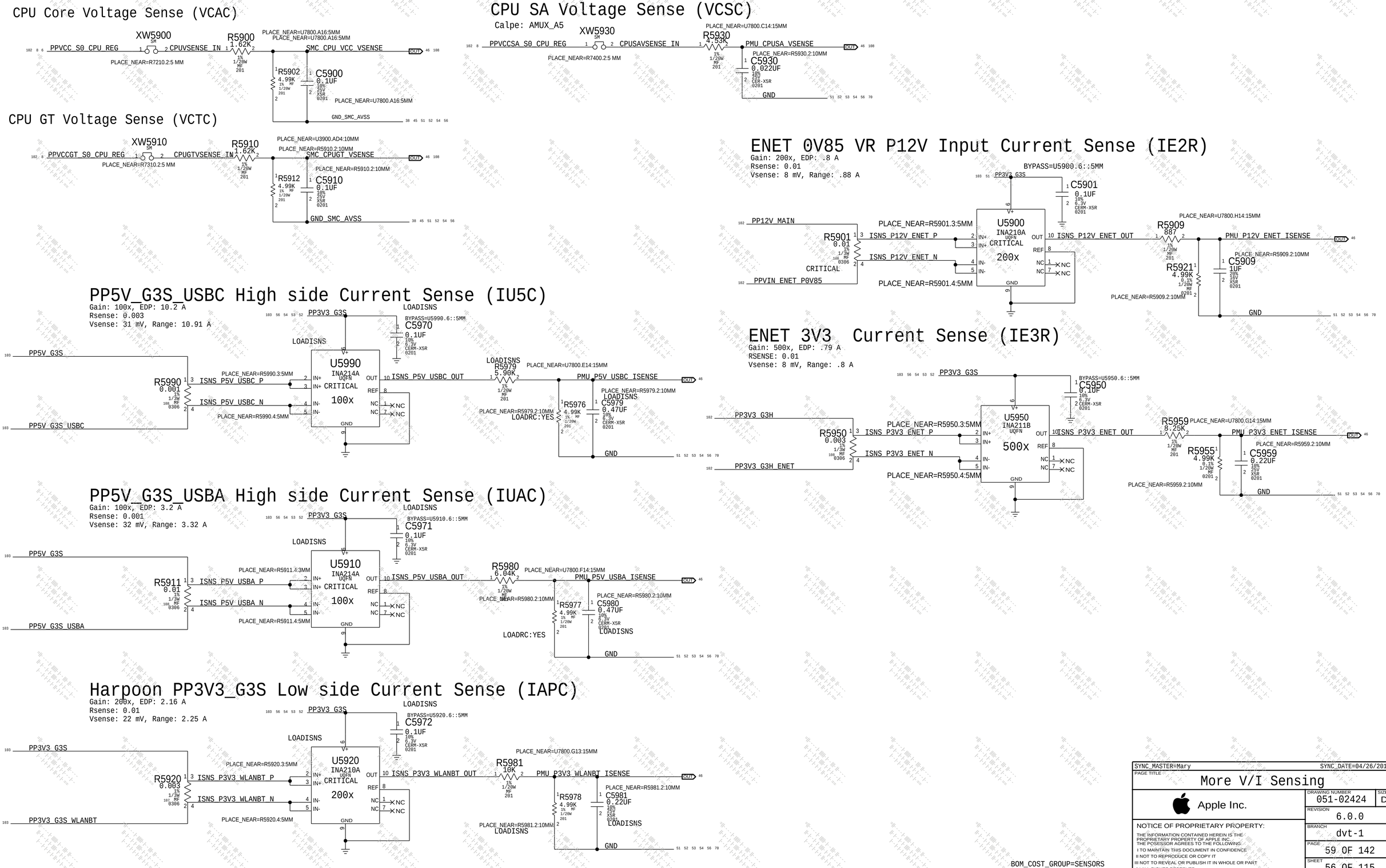

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: More V/I Sensing

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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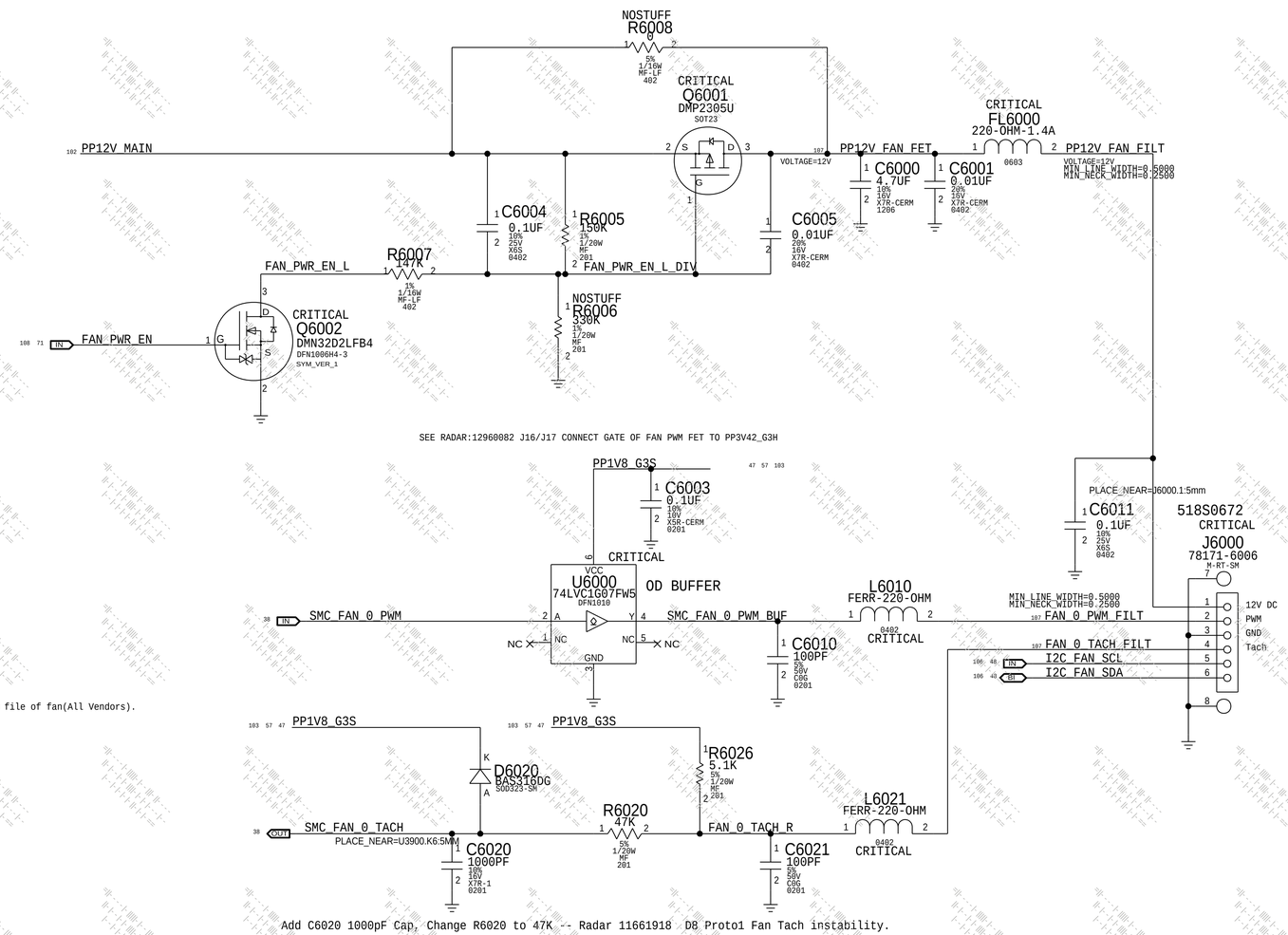
SMC Fan 0 (System)



Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).

Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

BOM_COST_GROUP=FAN

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	System Fan Connector
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
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SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SPI Debug Connector

Apple Inc.

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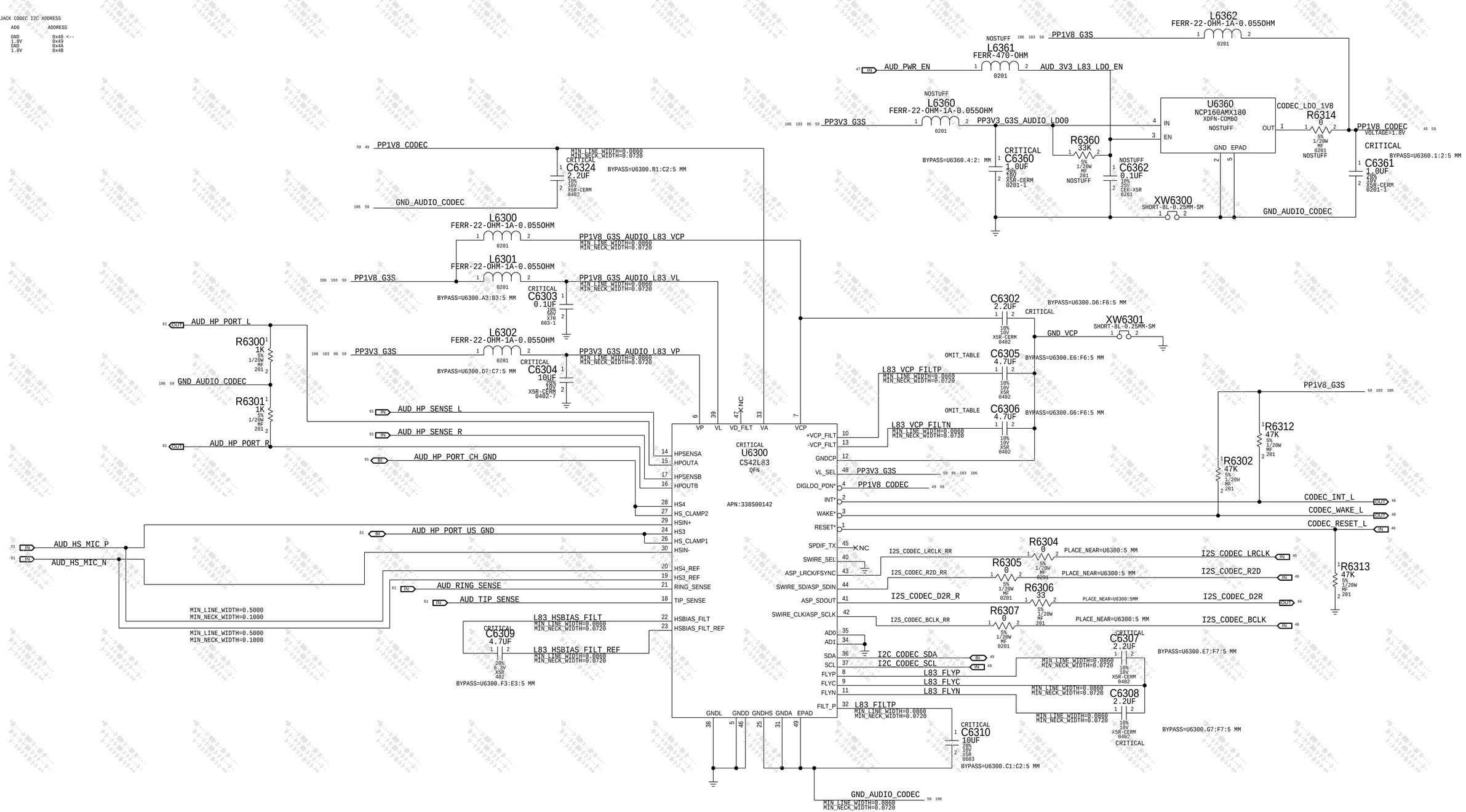
BOM_COST_GROUP=DEBUG

AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

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DRAWING NUMBER: 051-02424 SIZE: D

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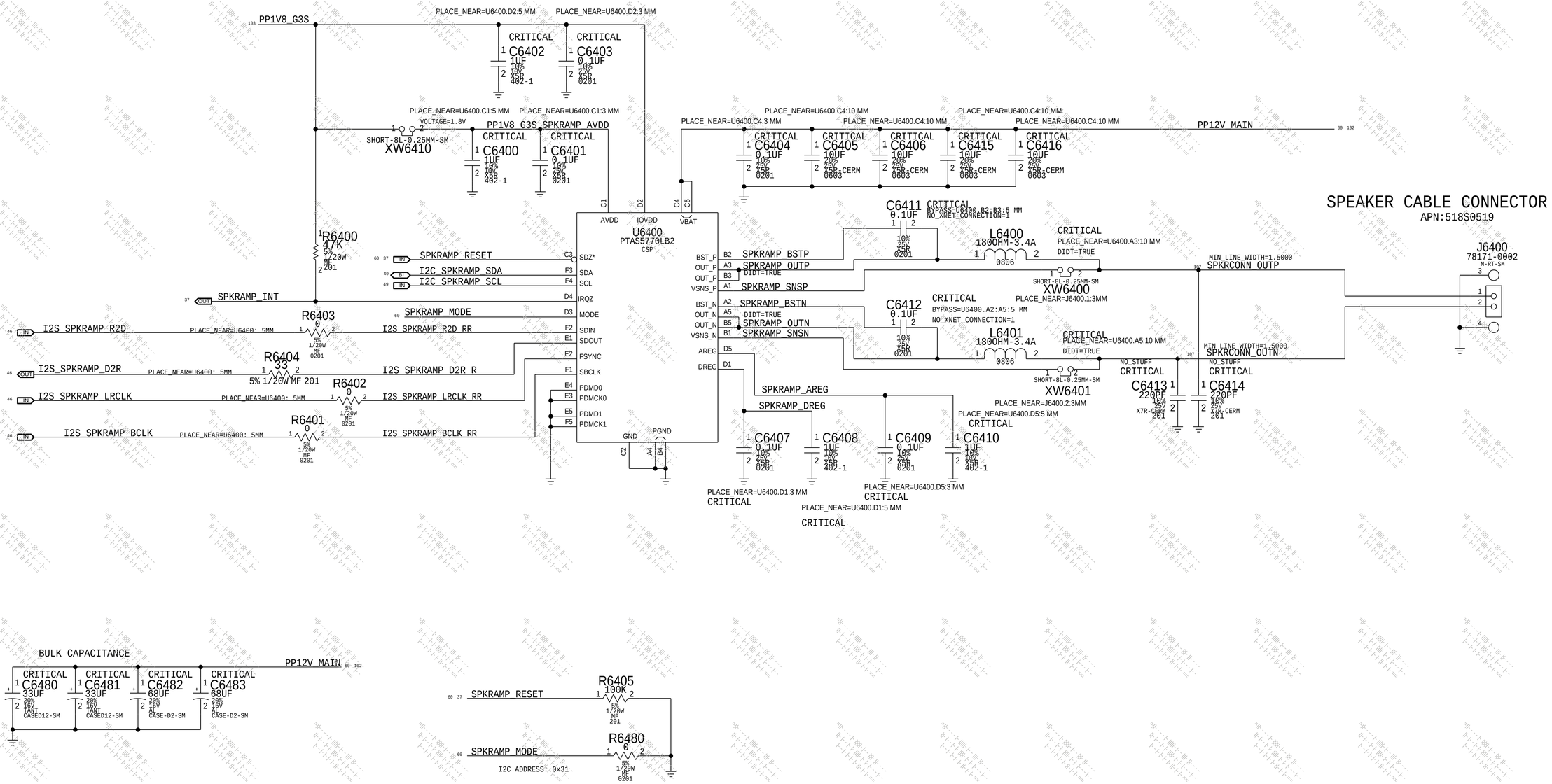
1x MONO SPEAKER AMPLIFIER (TAS5770)
APN: 353S01629



BOM_COST_GROUP=AUDIO

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: AUDIO SKPR AMP

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

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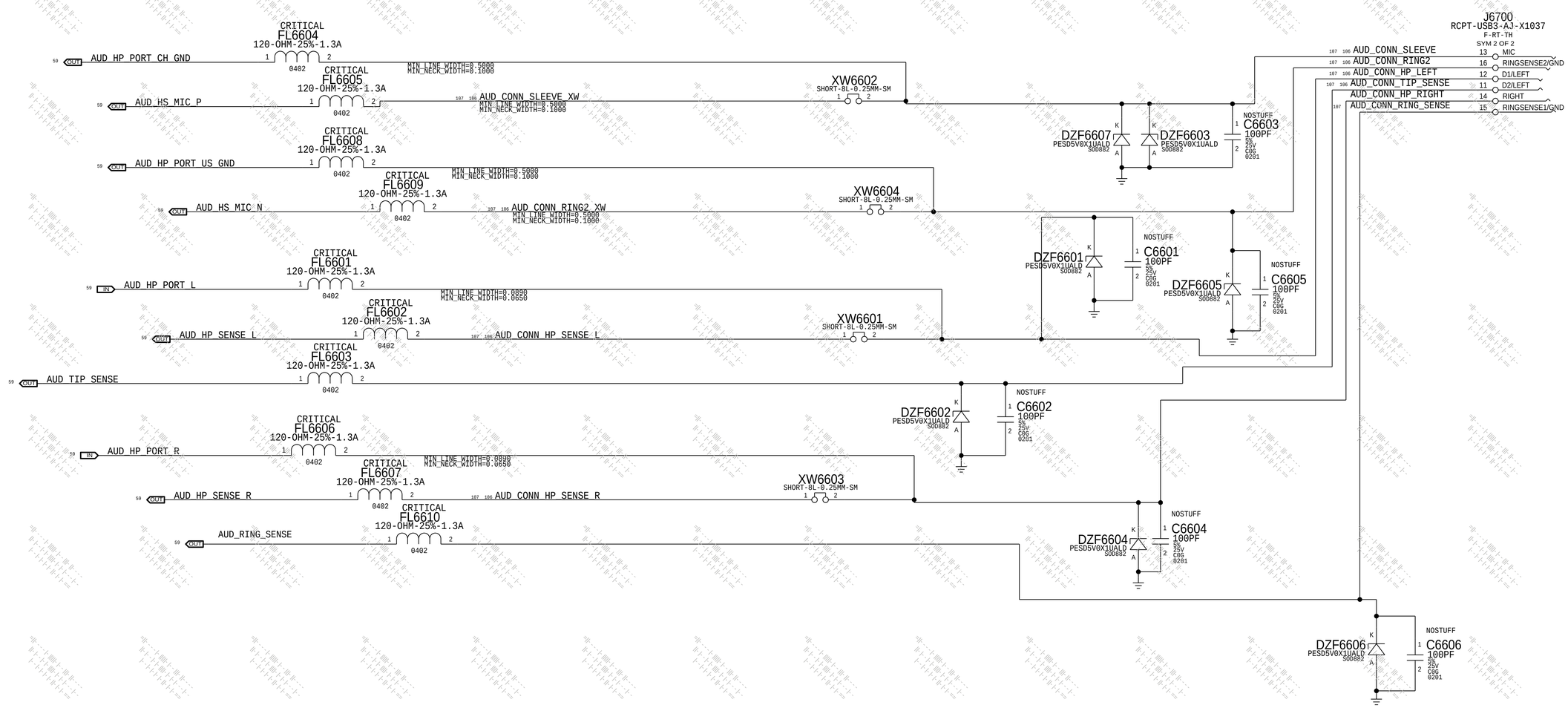

BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO JACK CONNECTOR

Apple Inc.

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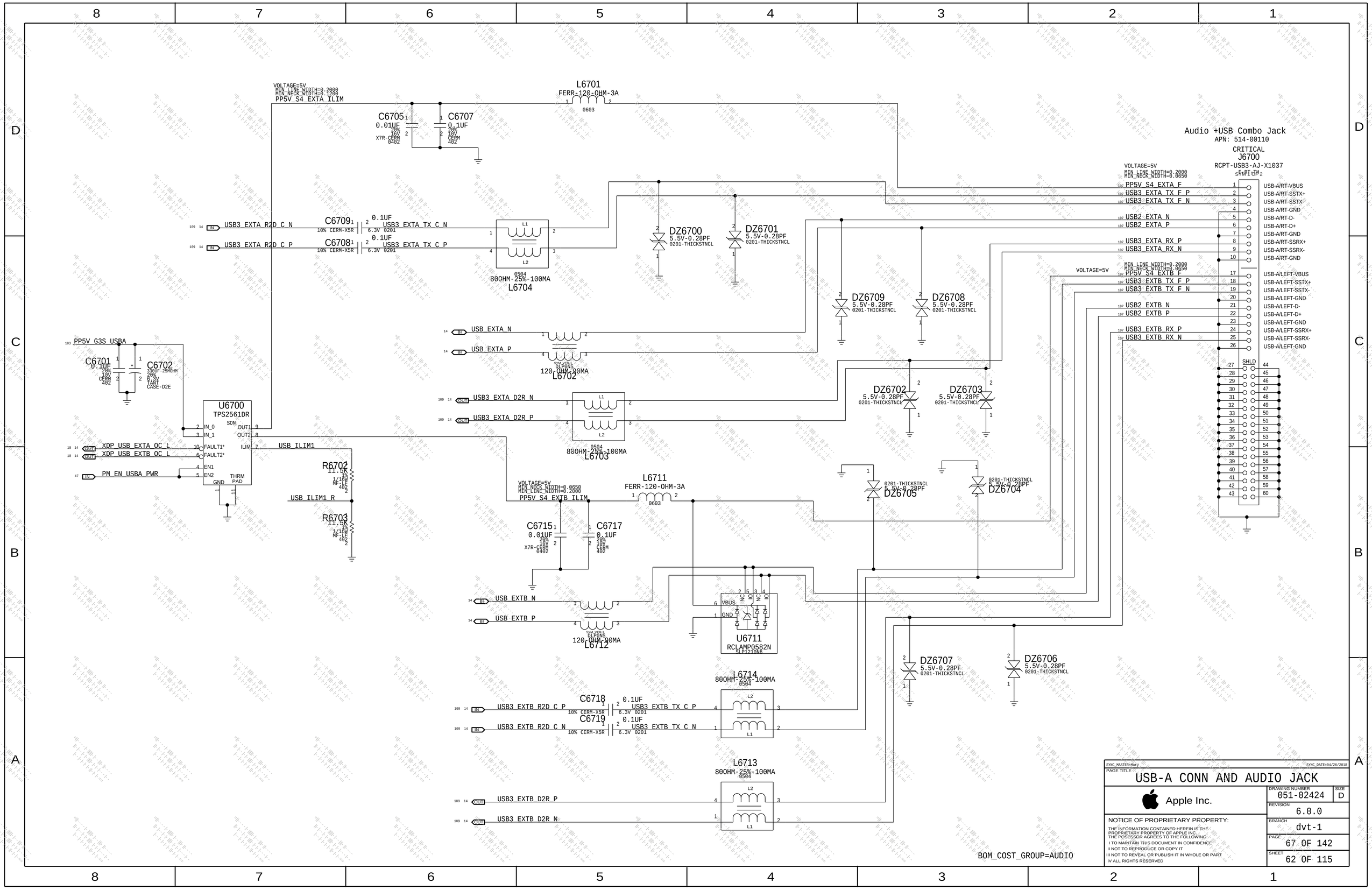
Audio +USB Combo Jack
APN: 514-00110
CRITICAL
J6700
RCPT-USB3-AJ-X1037
L6701
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
C6705
0.01UF
20%
16V
X7R-CERM
0402
C6707
0.1UF
20%
16V
CERM
402
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
C6709
C6708
0.1UF
10% CERM-X5R
6.3V 0201
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
L6704
80OHM-25%-100MA
0504
DZ6700
DZ6701
5.5V-0.28PF
0201-THICKSTNCL
DZ6709
DZ6708
PP5V_S4_EXTA_F
USB3_EXTA_TX_F_P
USB3_EXTA_TX_F_N
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_RX_P
USB3_EXTA_RX_N
USB-A/RT-VBUS
USB-A/RT-SSTX+
USB-A/RT-SSTX-
USB-A/RT-GND
USB-A/RT-D-
USB-A/RT-D+
USB-A/RT-GND
USB-A/RT-SSRX+
USB-A/RT-SSRX-
USB-A/RT-GND
PP5V_S4_EXTB_F
USB3_EXTB_TX_F_P
USB3_EXTB_TX_F_N
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_RX_P
USB3_EXTB_RX_N
USB-A/LEFT-VBUS
USB-A/LEFT-SSTX+
USB-A/LEFT-SSTX-
USB-A/LEFT-GND
USB-A/LEFT-D-
USB-A/LEFT-D+
USB-A/LEFT-GND
USB-A/LEFT-SSRX+
USB-A/LEFT-SSRX-
USB-A/LEFT-GND
SHLD
PP5V_G3S_USBA
C6701
0.1UF
20%
16V
CERM
402
C6702
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
U6700
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
GND
THRM PAD
OUT1
OUT2
ILIM
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
PM_EN_USBA_PWR
USB_ILIM1
R6702
11.5K
1%
1/16W
MF-LF
402
USB_ILIM1_R
R6703
USB_EXTA_N
USB_EXTA_P
L6702
120-OHM-90MA
DLP0NS
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
L6703
DZ6702
DZ6703
DZ6705
DZ6704
0201-THICKSTNCL
L6711
FERR-120-OHM-3A
PP5V_S4_EXTB_ILIM
C6715
C6717
USB_EXTB_N
USB_EXTB_P
L6712
U6711
RCLAMP0582N
SLP1210N6
VBUS
GND
NC
IO
DZ6707
DZ6706
L6714
L6713
USB3_EXTB_R2D_C_P
USB3_EXTB_R2D_C_N
C6718
C6719
USB3_EXTB_TX_C_P
USB3_EXTB_TX_C_N
USB3_EXTB_D2R_P
USB3_EXTB_D2R_N
BOM_COST_GROUP=AUDIO
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-A CONN AND AUDIO JACK
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
PAGE
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SHEET
62 OF 115
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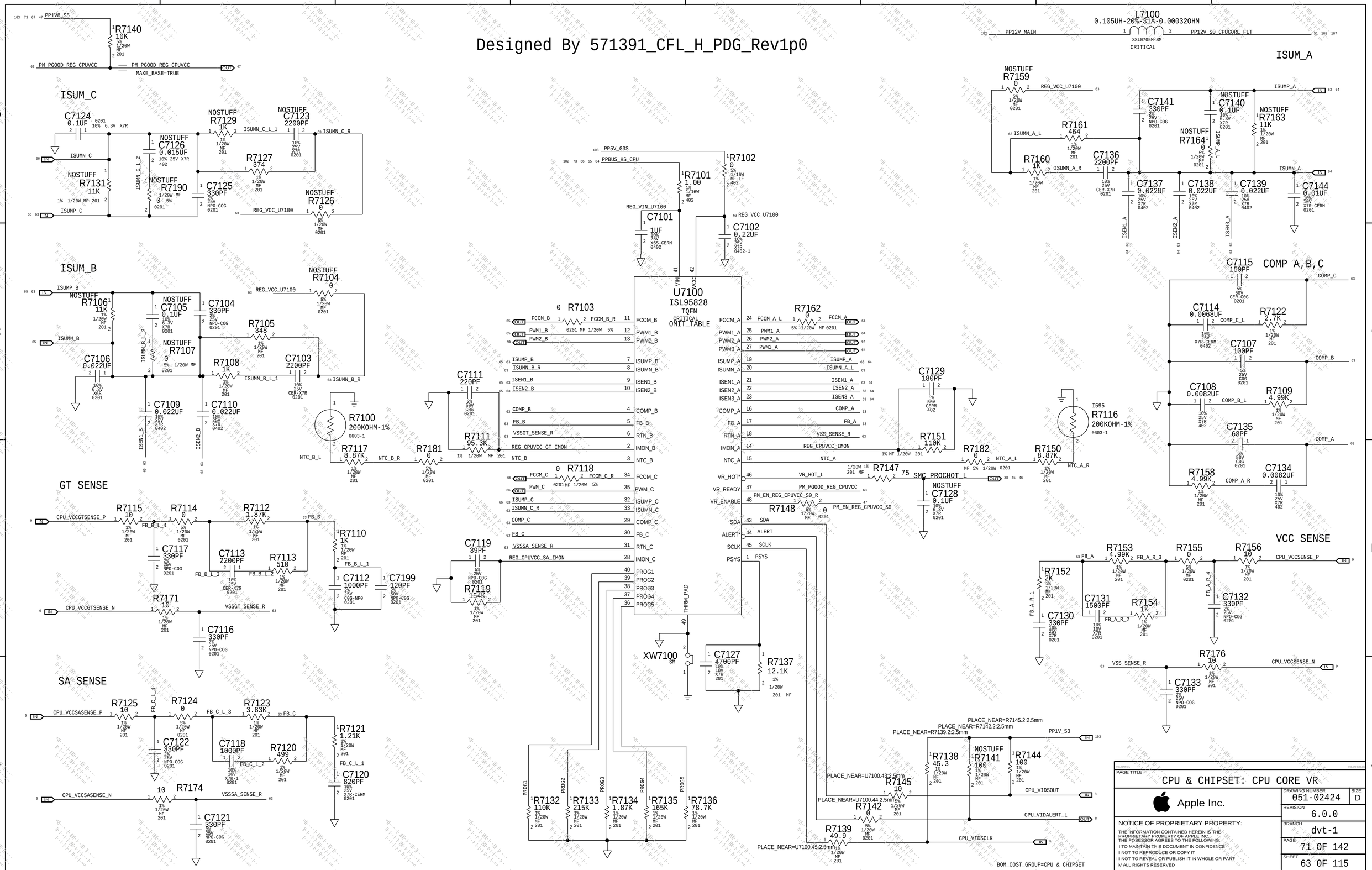

PAGE TITLE

CPU & CHIPSET: CPU CORE VR

Apple Inc.

DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

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SHEET 63 OF 115

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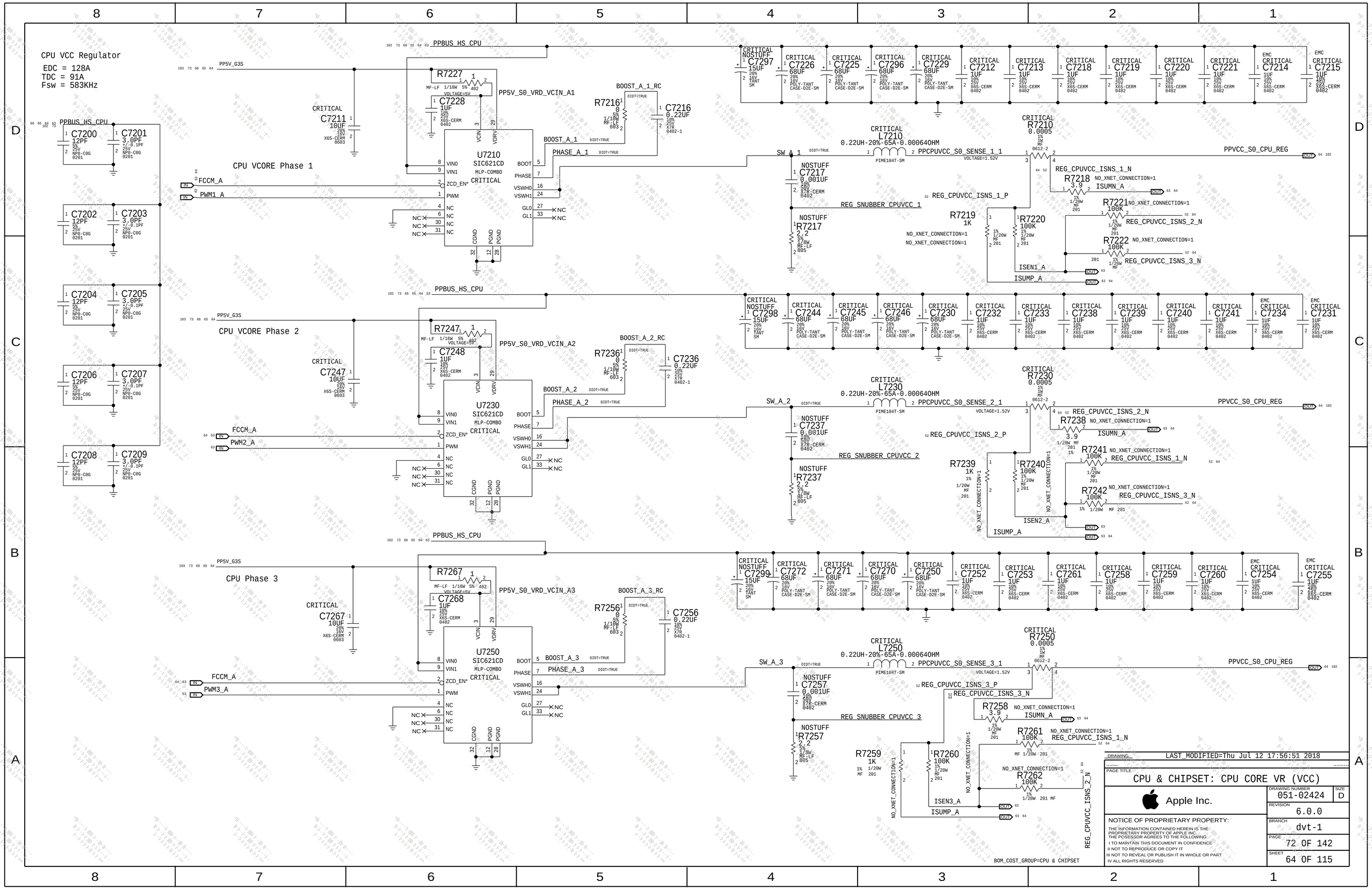

DRAWING: LAST_MODIFIED=Thu Jul 12 17:56:51 2018

PAGE TITLE: CPU & CHIPSET: CPU CORE VR (VCC)

Apple Inc.

DRAWING NUMBER: 051-02424 | SIZE: D

REVISION: 6.0.0

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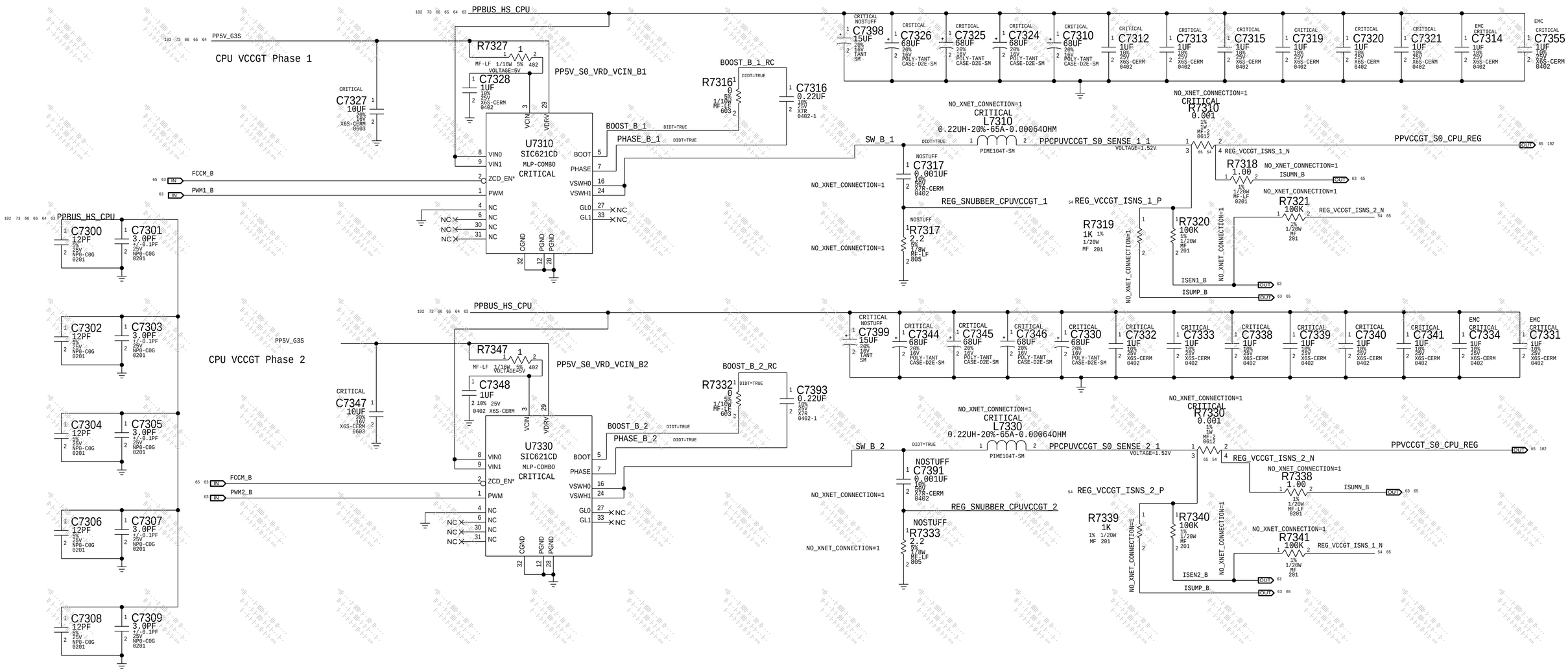
CPU VCCGT Regulator

EDC = 32A

TDC = 25A

Fsw = 583KHz



DRAWING	LAST_MODIFIED=Thu Jul 12 17:57:07 2018
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCGT)
	Apple Inc.
DRAWING NUMBER	051-02424
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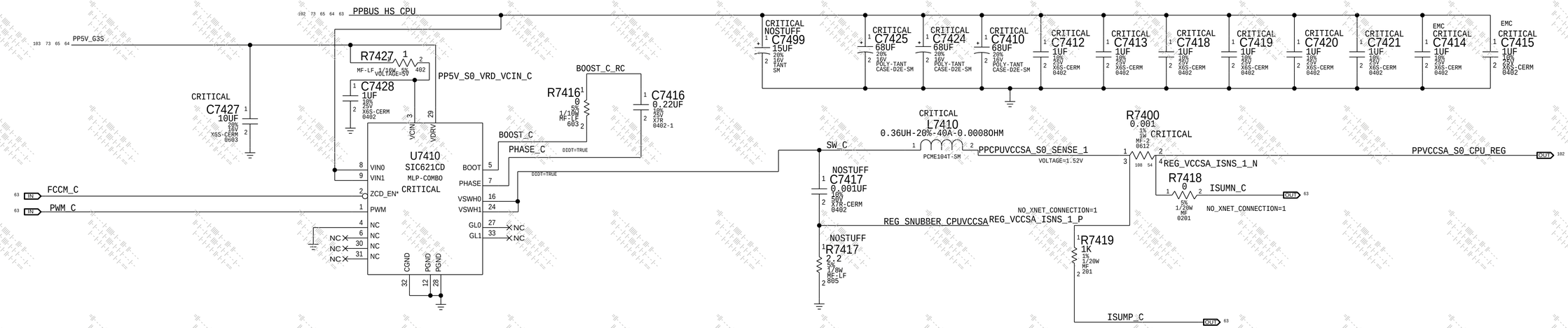
BOM_COST_GROUP=CPU & CHIPSET

CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A

Fsw = 583KHz



BOM_COST_GROUP=CPU & CHIPSET

DRAWING	LAST_MODIFIED=Thu Jul 12 17:57:07 2018
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCSA)
	Apple Inc.
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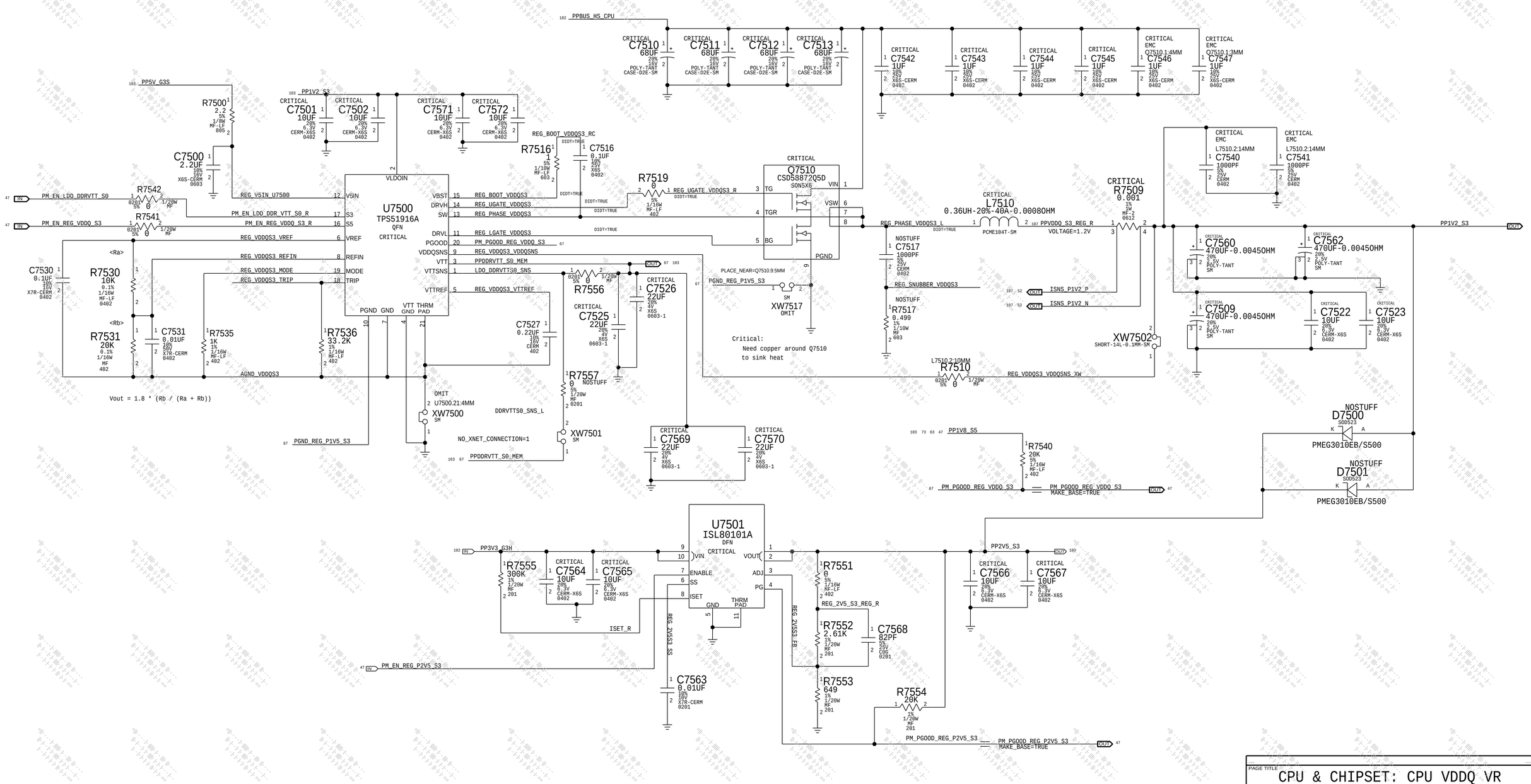
VDDQ S3 REGULATOR

VDDQ = 1.2V @ 8.43A (EDC)

VTT = 0.6V @ 1A (EDC)

VPP = 2.5V @ 0.384A (EDC)

Fsw = 500KHz



PAGE TITLE: CPU & CHIPSET: CPU VDDQ VR

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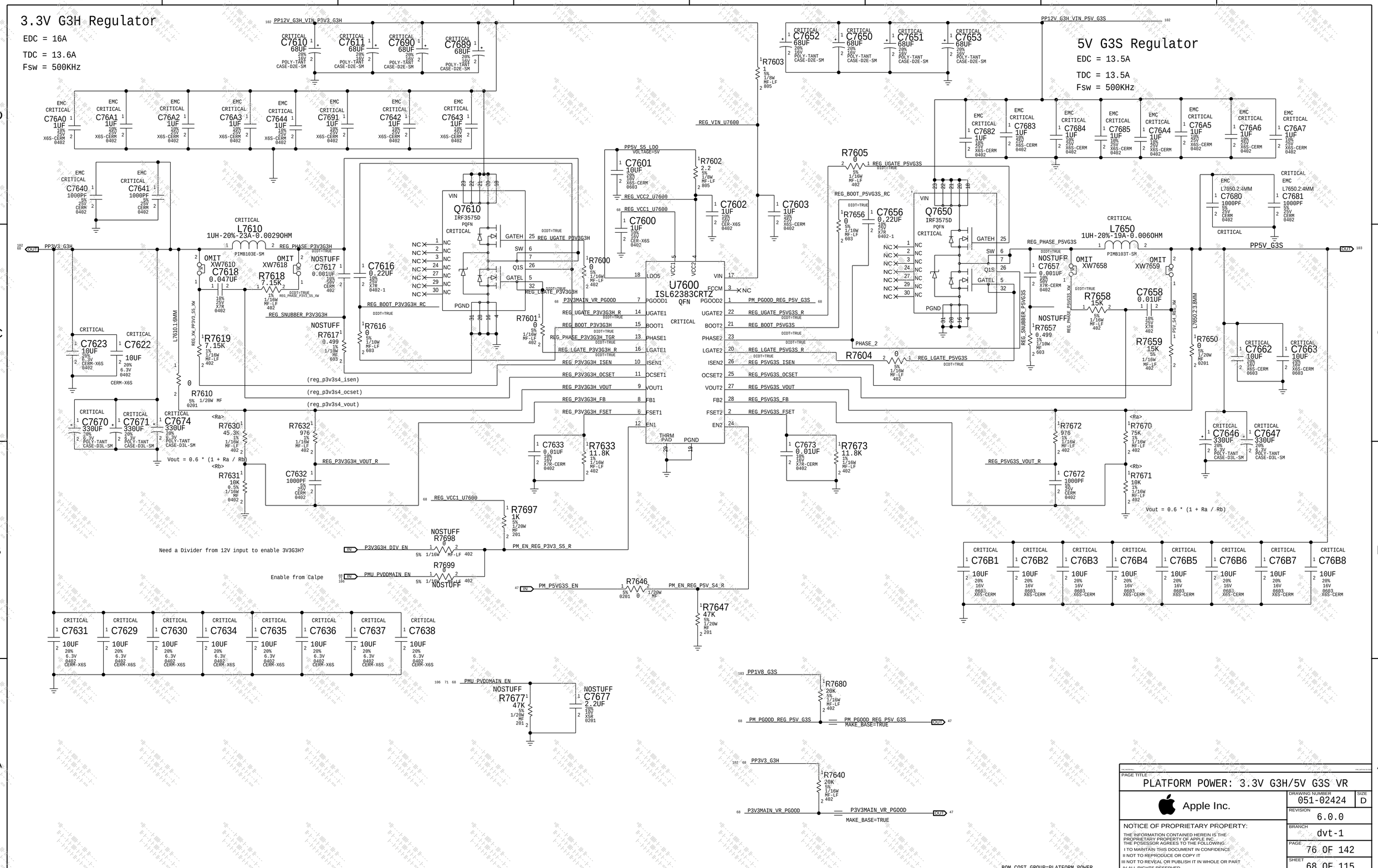
3.3V G3H Regulator
EDC = 16A
TDC = 13.6A
Fsw = 500KHz
5V G3S Regulator
EDC = 13.5A
TDC = 13.5A
Fsw = 500KHz
U7600
ISL62383CRTZ
QFN
Q7610
IRF3575D
Q7650
IRF3575D
L7610
1UH-20%-23A-0.0029OHM
L7650
1UH-20%-19A-0.0060HM
Vout = 0.6 * (1 + Ra / Rb)
Need a Divider from 12V input to enable 3V3G3H?
Enable from Calpe
PP3V3_G3H
PP5V_G3S
PP12V_G3H_VIN_P3V3_G3H
PP12V_G3H_VIN_P5V_G3S
PP1V8_G3S
PM_PGOOD_REG_P5V_G3S
P3V3MAIN_VR_PGOOD
PM_PGOOD_REG_P5V_G3S
MAKE_BASE=TRUE
BOM_COST_GROUP=PLATFORM POWER
PAGE TITLE
PLATFORM POWER: 3.3V G3H/5V G3S VR
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
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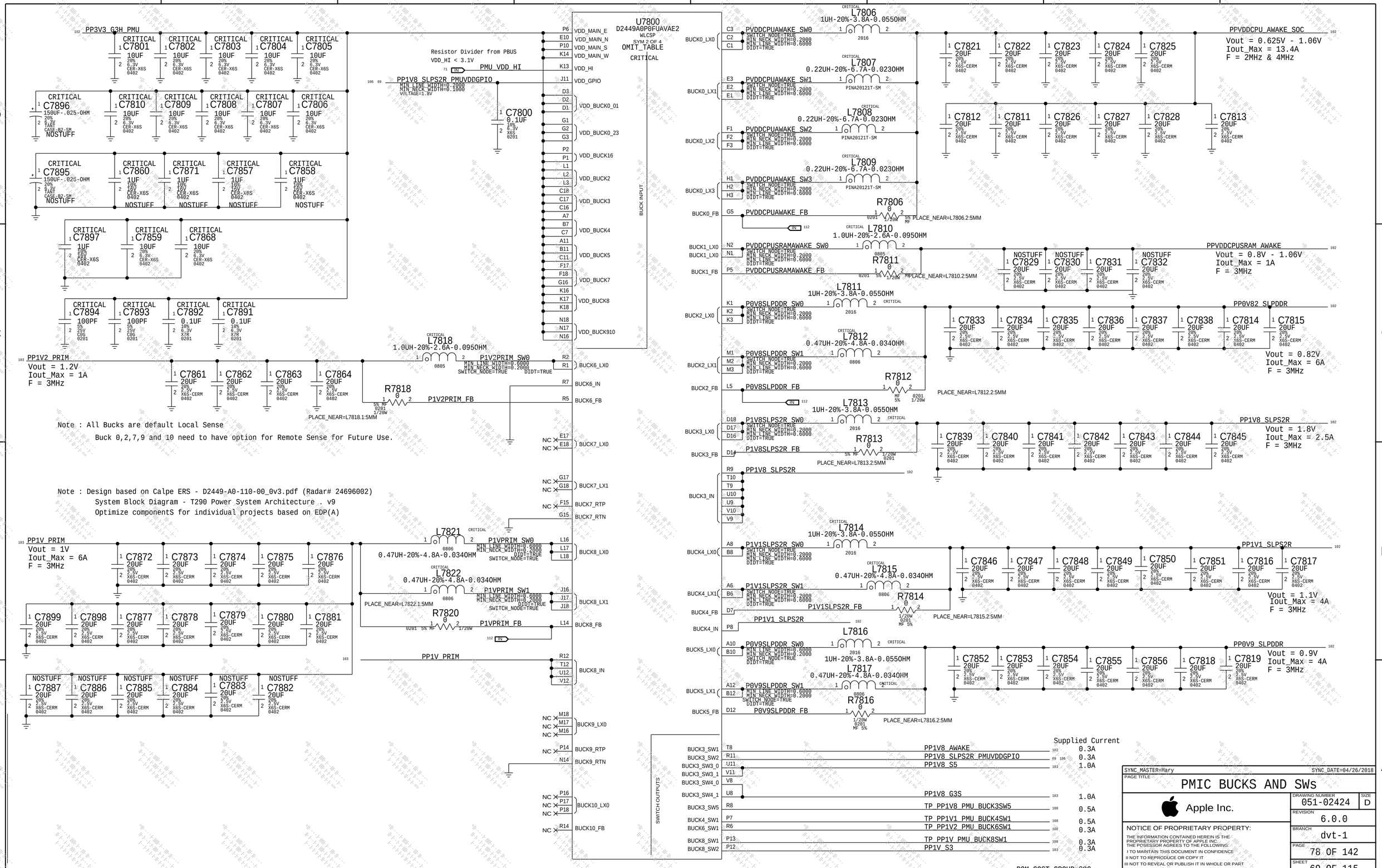
U7800
D2449A0P0FUAVAE2
WLCSP
SYM 2 OF 4
OMIT_TABLE
CRITICAL
BUCK INPUT
PP3V3_G3H_PMU
Resistor Divider from PBUS
VDD_HI < 3.1V
PMU_VDD_HI
PP1V8_SLPS2R_PMUVDDGPIO
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
VDD_MAIN_E
VDD_MAIN_N
VDD_MAIN_S
VDD_MAIN_W
VDD_HI
VDD_GPIO
VDD_BUCK0_01
VDD_BUCK0_23
VDD_BUCK16
VDD_BUCK2
VDD_BUCK3
VDD_BUCK4
VDD_BUCK5
VDD_BUCK7
VDD_BUCK8
VDD_BUCK910
PP1V2_PRIM
Vout = 1.2V
Iout_Max = 1A
F = 3MHz
L7818
1.0UH-20%-2.6A-0.095OHM
P1V2PRIM_SW0
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE
R7818
P1V2PRIM_FB
PLACE_NEAR=L7818.1:5MM
BUCK6_LX0
BUCK6_IN
BUCK6_FB
BUCK7_LX0
BUCK7_LX1
BUCK7_RTP
BUCK7_RTN
Note : All Bucks are default Local Sense
Buck 0,2,7,9 and 10 need to have option for Remote Sense for Future Use.
Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)
PP1V_PRIM
Vout = 1V
Iout_Max = 6A
F = 3MHz
L7821
0.47UH-20%-4.8A-0.034OHM
P1VPRIM_SW0
L7822
0.47UH-20%-4.8A-0.034OHM
P1VPRIM_SW1
PLACE_NEAR=L7822.1:5MM
R7820
P1VPRIM_FB
BUCK8_LX0
BUCK8_LX1
BUCK8_FB
BUCK8_IN
BUCK9_LX0
BUCK9_RTP
BUCK9_RTN
BUCK10_LX0
BUCK10_FB
L7806
1UH-20%-3.8A-0.055OHM
PVDDCPUAWAKE_SW0
PPVDDCPU_AWAKE_SOC
Vout = 0.625V - 1.06V
Iout_Max = 13.4A
F = 2MHz & 4MHz
L7807
0.22UH-20%-6.7A-0.023OHM
PVDDCPUAWAKE_SW1
L7808
0.22UH-20%-6.7A-0.023OHM
PVDDCPUAWAKE_SW2
L7809
0.22UH-20%-6.7A-0.023OHM
PVDDCPUAWAKE_SW3
R7806
PVDDCPUAWAKE_FB
PLACE_NEAR=L7806.2:5MM
L7810
1.0UH-20%-2.6A-0.095OHM
PVDDCPUSRAMAWAKE_SW0
PPVDDCPUSRAM_AWAKE
Vout = 0.8V - 1.06V
Iout_Max = 1A
F = 3MHz
R7811
PVDDCPUSRAMAWAKE_FB
PLACE_NEAR=L7810.2:5MM
L7811
1UH-20%-3.8A-0.055OHM
P0V8SLPDDR_SW0
PP0V82_SLPDDR
Vout = 0.82V
Iout_Max = 6A
F = 3MHz
L7812
0.47UH-20%-4.8A-0.034OHM
P0V8SLPDDR_SW1
R7812
P0V8SLPDDR_FB
PLACE_NEAR=L7812.2:5MM
L7813
1UH-20%-3.8A-0.055OHM
P1V8SLPS2R_SW0
PP1V8_SLPS2R
Vout = 1.8V
Iout_Max = 2.5A
F = 3MHz
R7813
P1V8SLPS2R_FB
PLACE_NEAR=L7813.2:5MM
PP1V8_SLPS2R
L7814
1UH-20%-3.8A-0.055OHM
P1V1SLPS2R_SW0
PP1V1_SLPS2R
Vout = 1.1V
Iout_Max = 4A
F = 3MHz
L7815
0.47UH-20%-4.8A-0.034OHM
P1V1SLPS2R_SW1
R7814
P1V1SLPS2R_FB
PLACE_NEAR=L7815.2:5MM
PP1V1_SLPS2R
L7816
1UH-20%-3.8A-0.055OHM
P0V9SLPDDR_SW0
PP0V9_SLPDDR
Vout = 0.9V
Iout_Max = 4A
F = 3MHz
L7817
0.47UH-20%-4.8A-0.034OHM
P0V9SLPDDR_SW1
R7816
P0V9SLPDDR_FB
PLACE_NEAR=L7816.2:5MM
SWITCH OUTPUTS
Supplied Current
BUCK3_SW1 PP1V8_AWAKE 0.3A
BUCK3_SW2 PP1V8_SLPS2R_PMUVDDGPIO 0.3A
BUCK3_SW3_0 PP1V8_S5 1.0A
BUCK3_SW4_1 PP1V8_G3S 1.0A
BUCK3_SW5 TP_PP1V8_PMU_BUCK3SW5 0.5A
BUCK4_SW1 TP_PP1V1_PMU_BUCK4SW1 0.5A
BUCK6_SW1 TP_PP1V2_PMU_BUCK6SW1 0.3A
BUCK8_SW1 TP_PP1V_PMU_BUCK8SW1 0.3A
BUCK8_SW2 PP1V_S3 0.3A
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
PMIC BUCKS AND SWs
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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SHEET 69 OF 115
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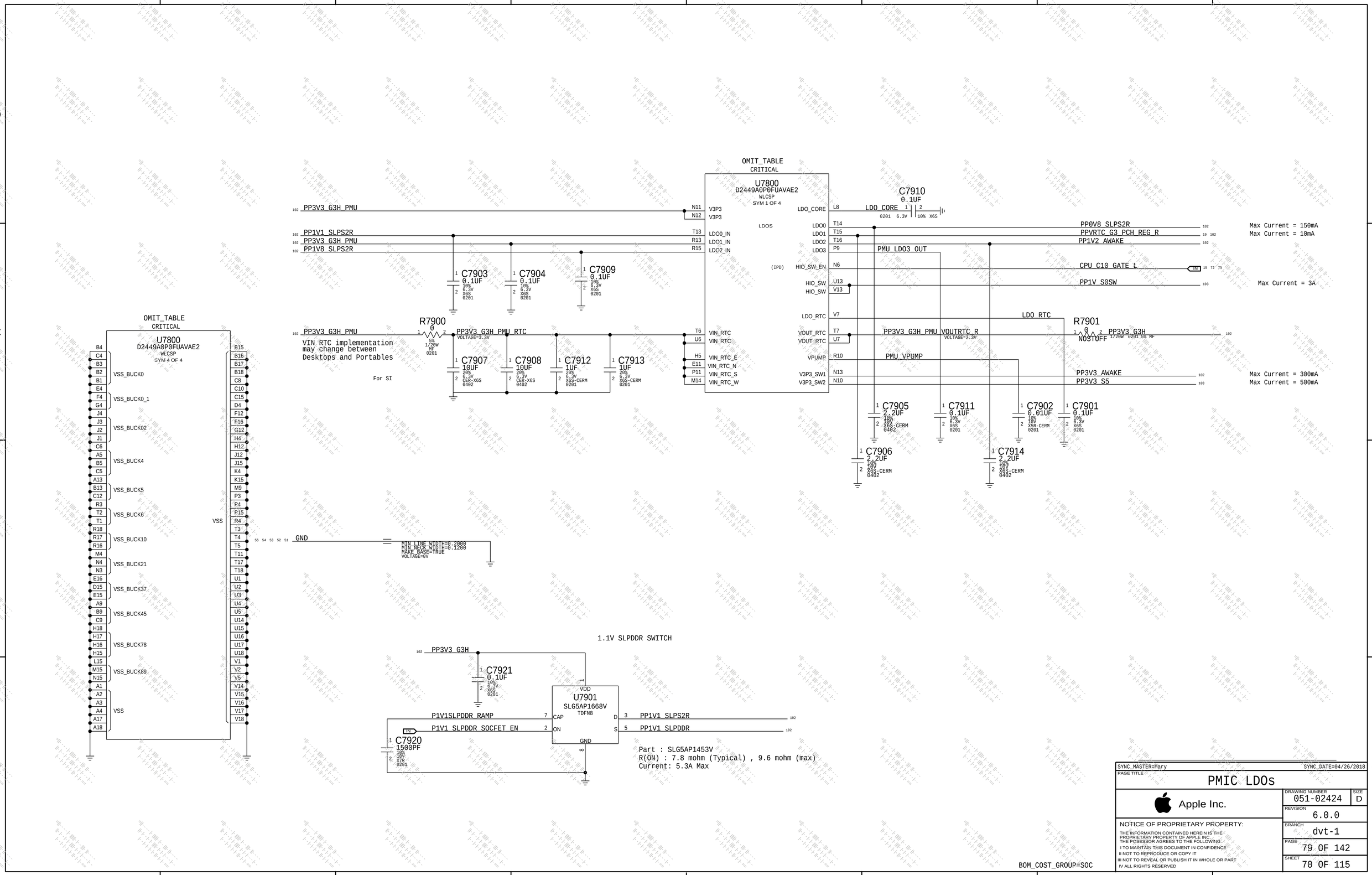

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: PMIC LDOs

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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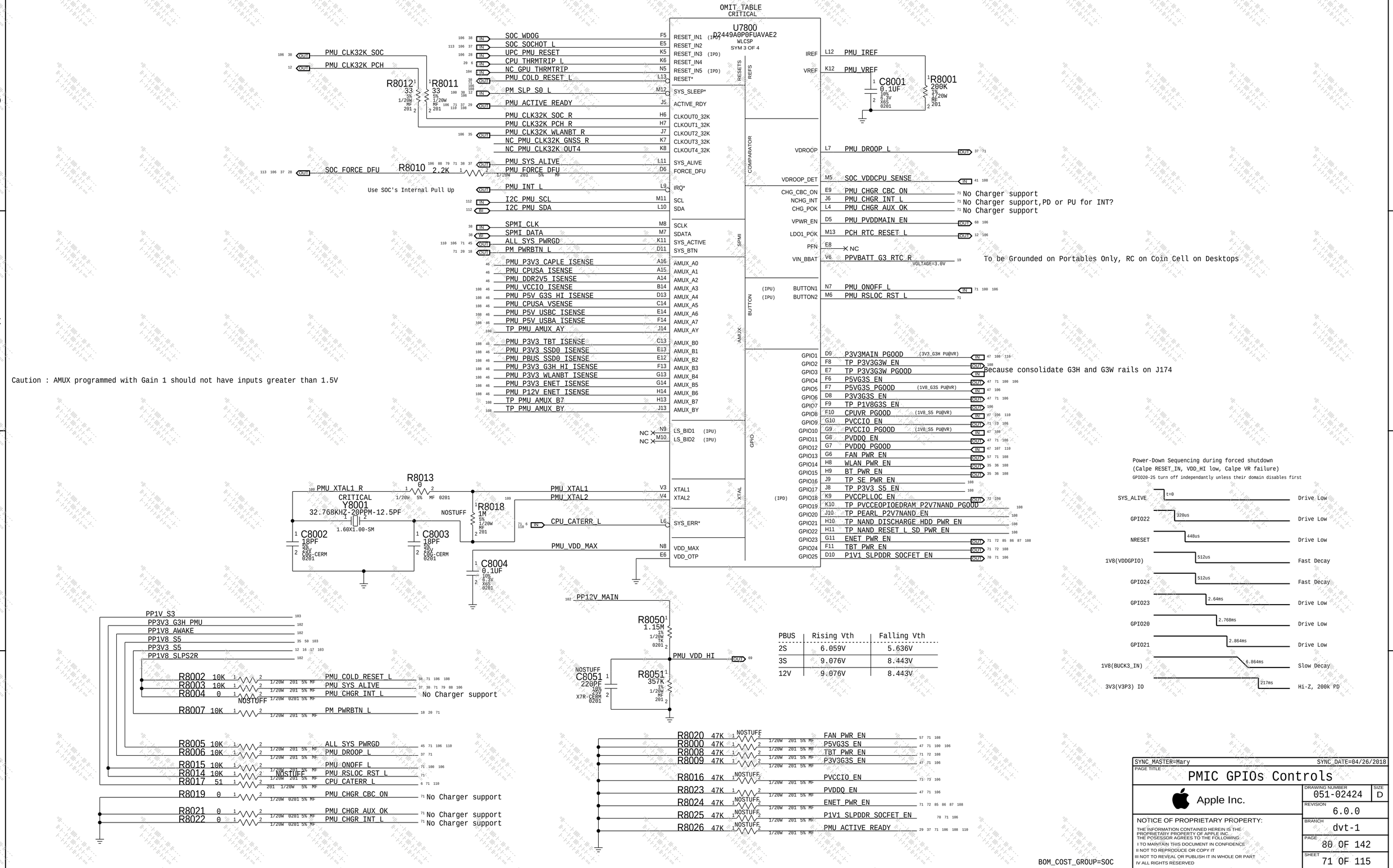


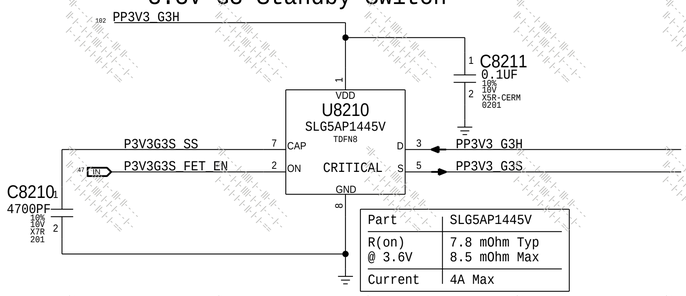
PBUS	Rising Vth	Falling Vth
2S	6.059V	5.636V
3S	9.076V	8.443V
12V	9.076V	8.443V

System Power States

System State:	Shutdown (G3H)		Standby (G3S)		Standby (S4)		Sleep (S0i/S3)		Run (S0)
CPU/PCH State:	Off (RTC Only)		Off (RTC Only)		Standby		Sleep		Run
Rails / SoC State:	S2R	Awake	S2R	Awake	S2R	Awake	S2R	Awake	Awake
PP*_S2R (0.8,1.1,1.8V)	On	On	On	On	On	On	On	On	On
PP*_DDR (0.8,0.9,1.1V)	Off	On	Off	On	Off	On	Off	On	On
PP*_AWAKE (CPU,SRAM,1.2,1.8,3.3V)	Off	On	Off	On	Off	On	Off	On	On
PP3V3_G3H (VR1)	On	On	On	On	On	On	On	On	On
PP1S_G3H	On	On	On	On	On	On	On	On	On
PP3V3_G3W	Off	On	Off	On	On	On	On	On	On
PP*_G3S (1.8,3.3,5V)	Off	On	On	On	On	On	On	On	On
PP*_S5 (1.8,3.3V)	Off	Off	Off	Off	On	On	On	On	On
CPU/PCH VRs	Off	Off	Off	Off	Off/On	Off/On	Off/On	Off/On	On

* System: Shutdown Awake is a transition state only.
* SoC: SLP_DDR is a transition state only.
* CPU/PCH: S4 is only used by desktops for USB wakes.
* CPU/PCH: S5 is a transition state. May also be used for RTC wakes.

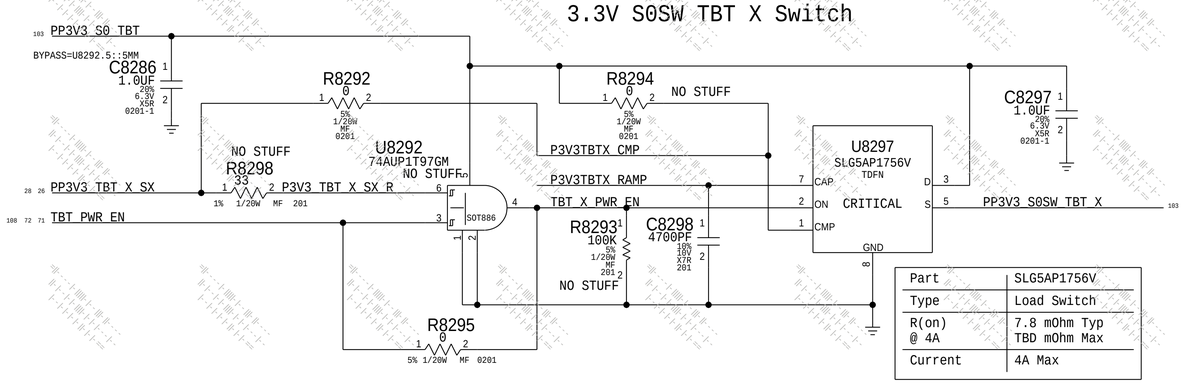
3.3V G3 Standby Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

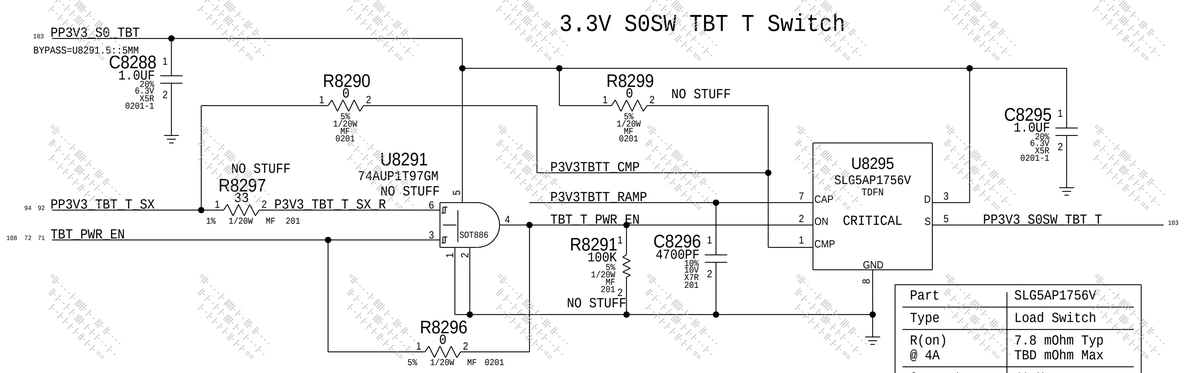
Based off rdar://30356539. 3V3_G3W can be combined into 3V3_G3H.

3.3V S0SW TBT X Switch



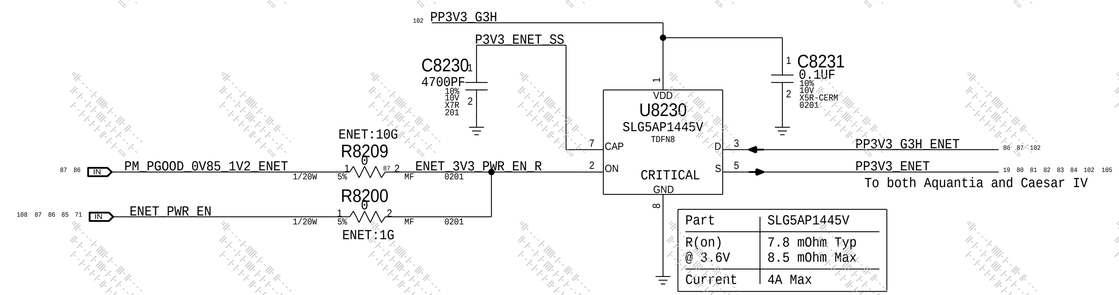
Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

3.3V S0SW TBT T Switch



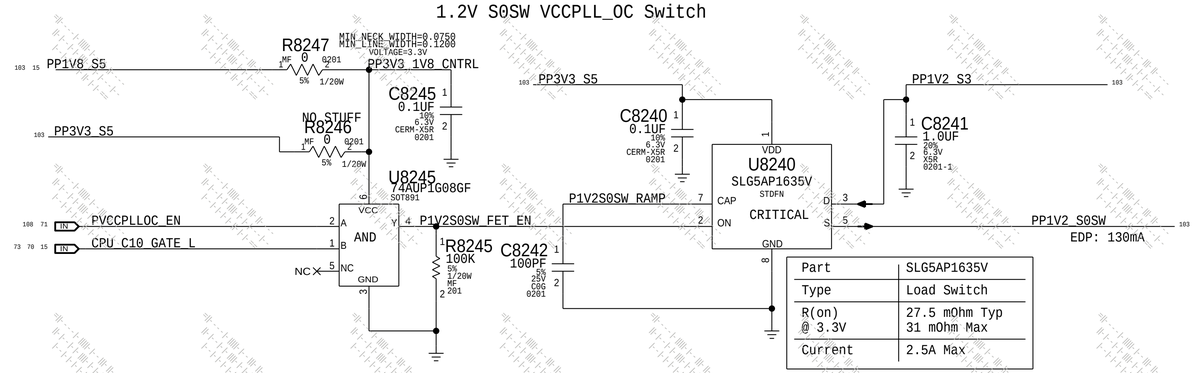
Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

3.3V ENET Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

1.2V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.3V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

VCCPLL_OC has turn-on requirement of 11uS min and 240uS max from EN to 1.1V

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power FETs

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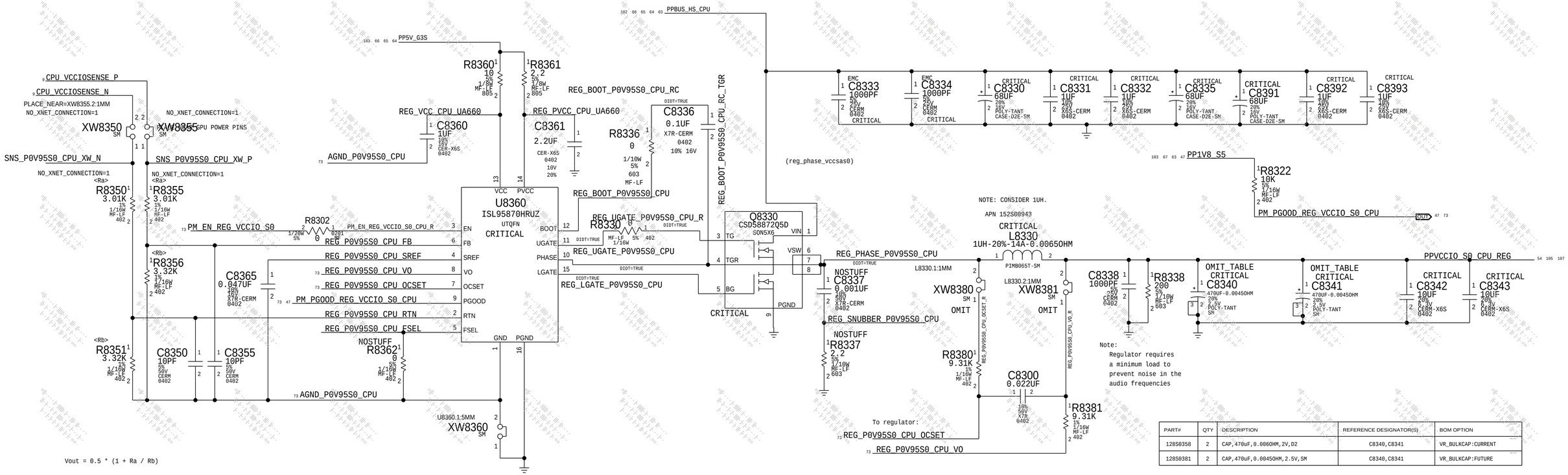
VCCIO S0 REGULATOR

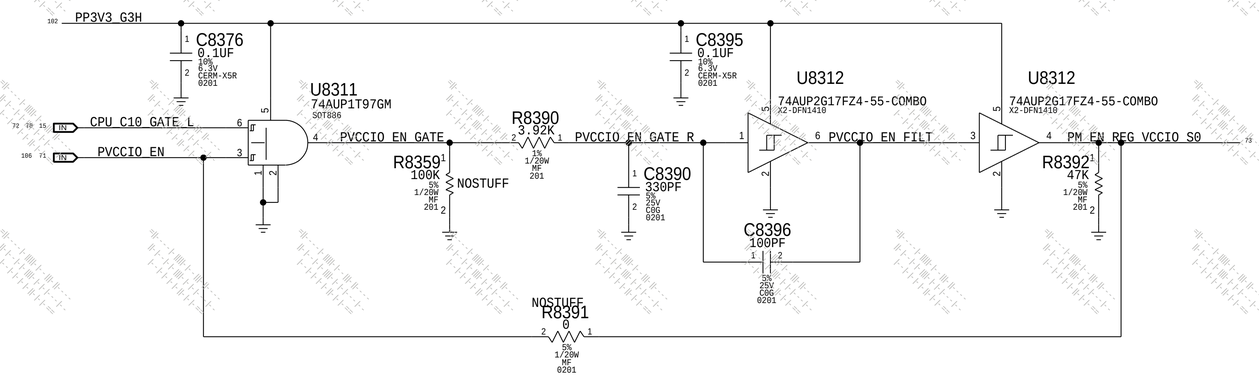
EDC = 6.4A

TDC = 6.4A

Fsw = 500KHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	C8340,C8341	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.00450HM,2.5V,SM	C8340,C8341	VR_BULKCAP:FUTURE



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DRAWING: LAST_MODIFIED=Thu Jul 12 17:57:13 2018

PAGE TITLE: CPU & CHIPSET: CPU VCCIO VR

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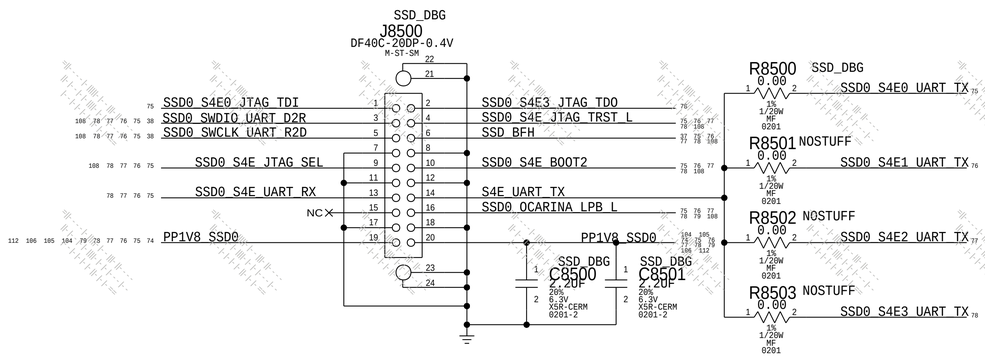

BOM_COST_GROUP=DEBUG

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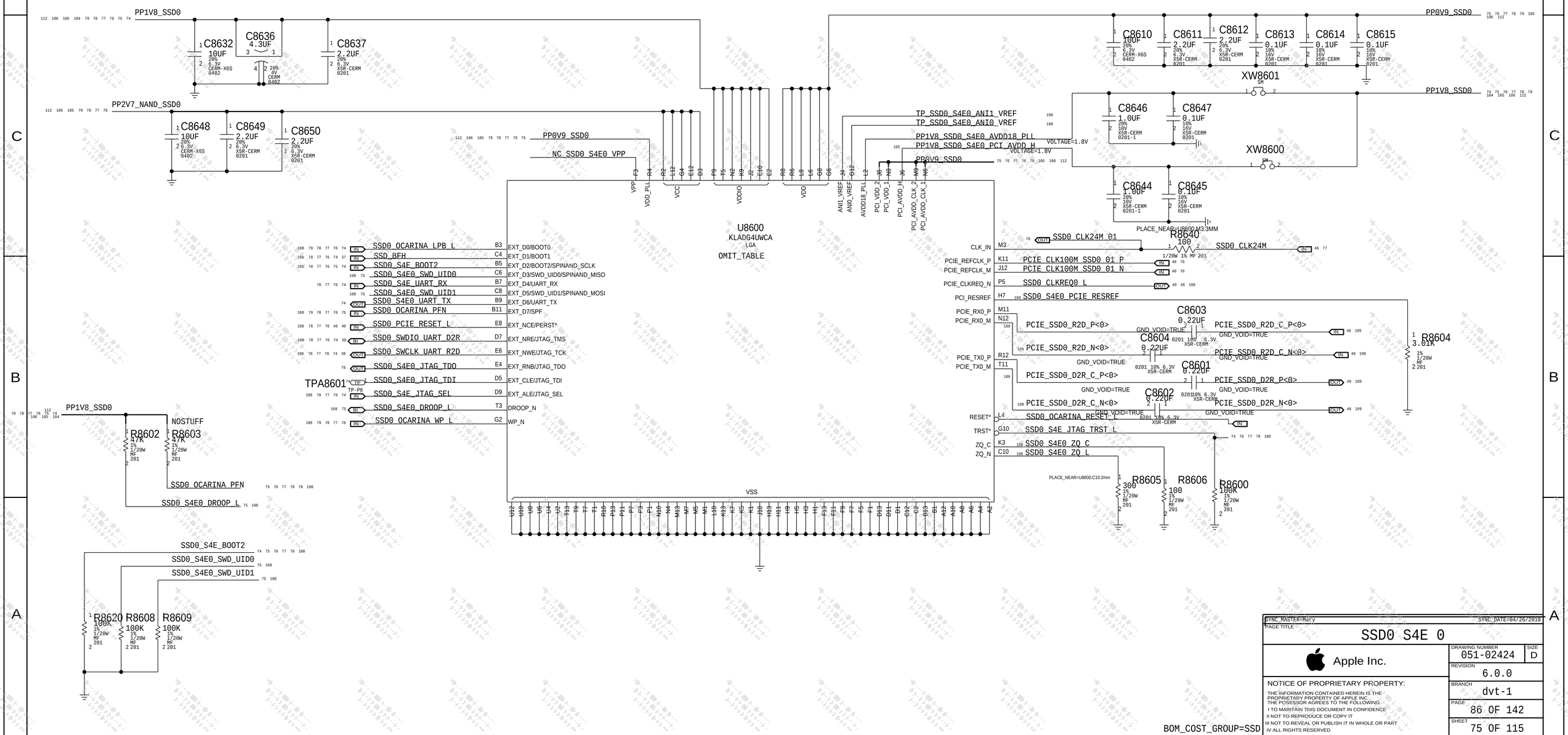
S4E0



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SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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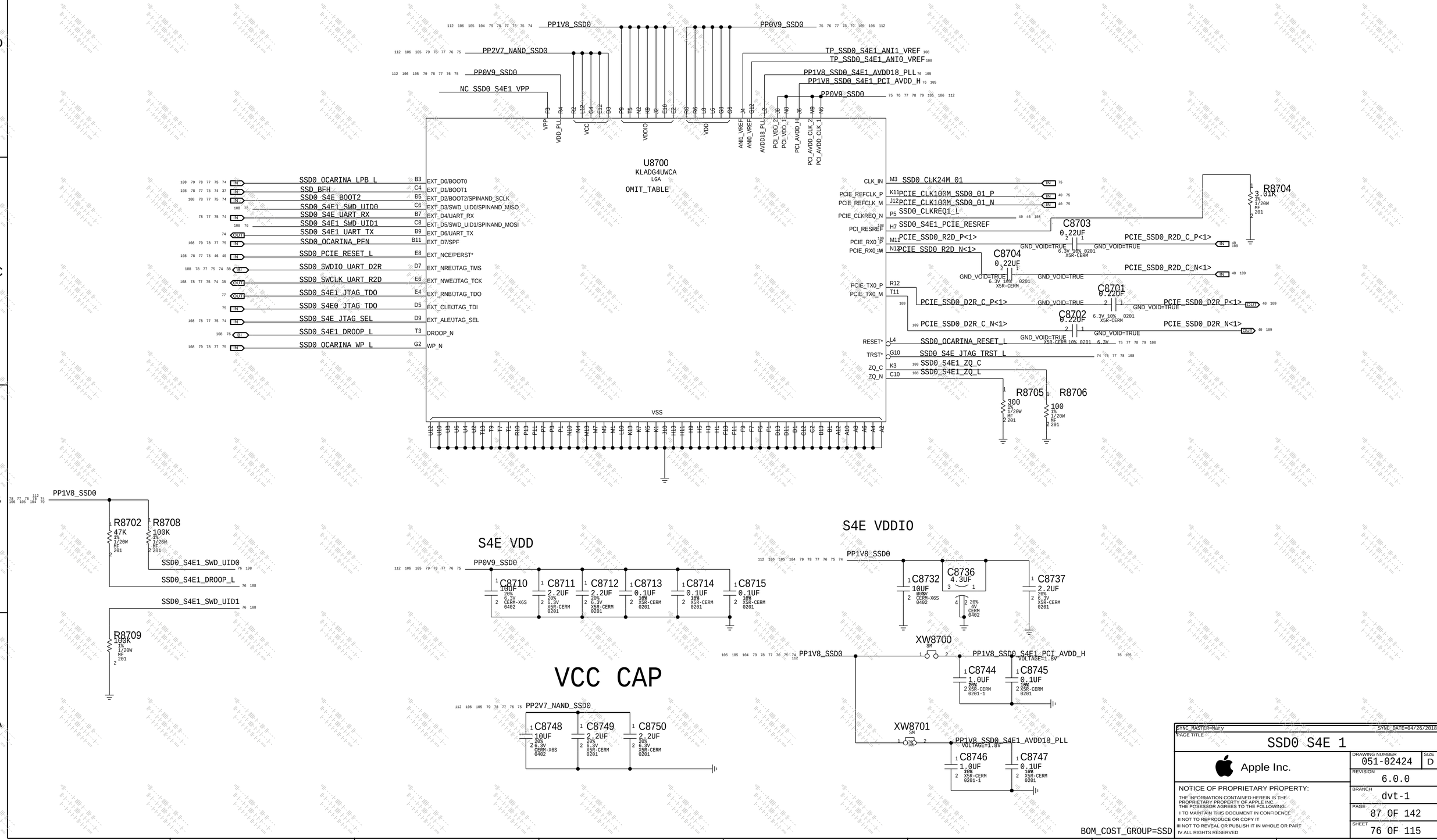

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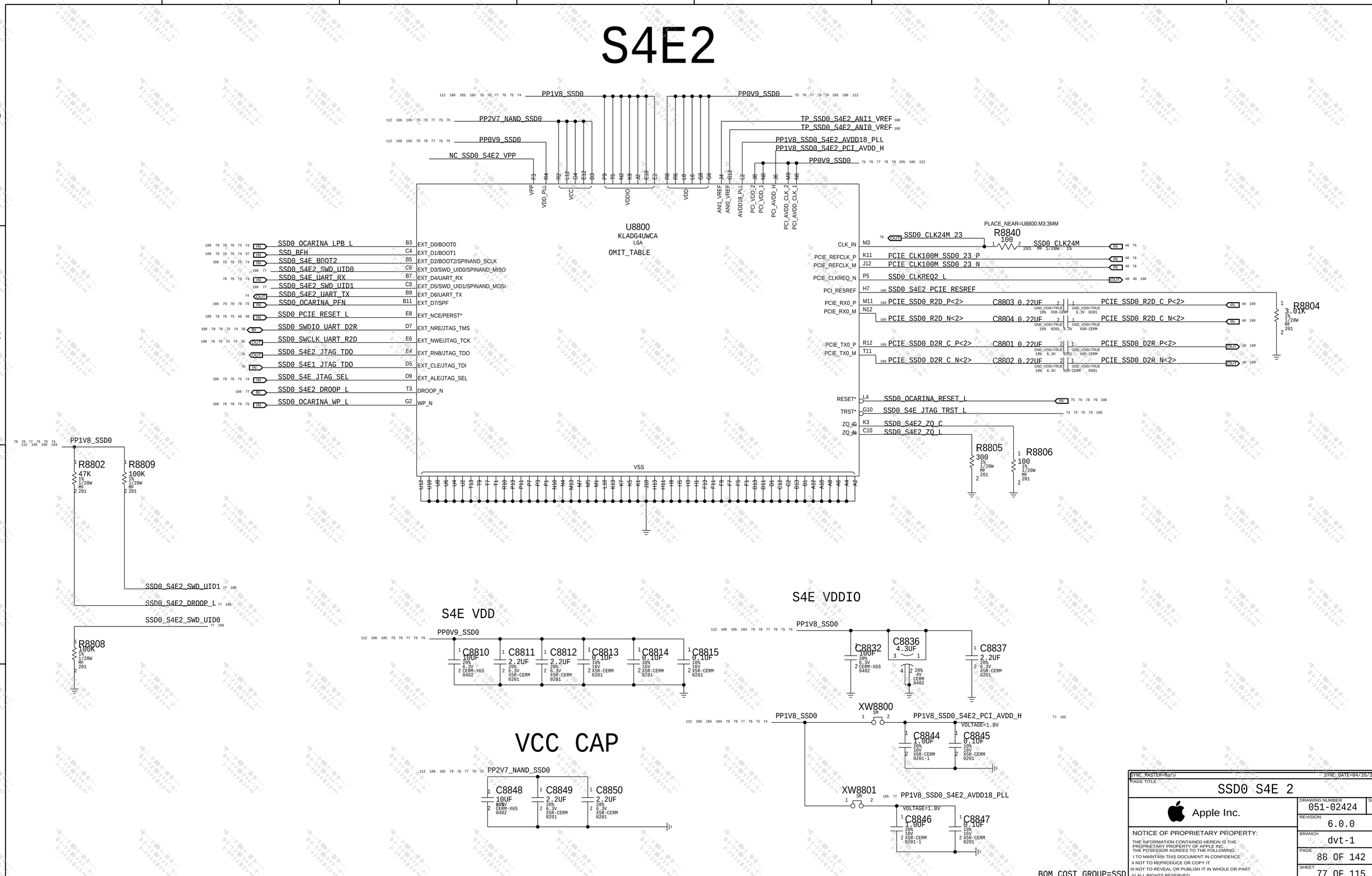
PP1V8_SSD0
PP0V9_SSD0
PP2V7_NAND_SSD0
PP0V9_SSD0
NC_SSD0_S4E2_VPP
TP_SSD0_S4E2_ANI1_VREF
TP_SSD0_S4E2_ANI0_VREF
PP1V8_SSD0_S4E2_AVDD18_PLL
PP1V8_SSD0_S4E2_PCI_AVDD_H
PP0V9_SSD0
U8800
KLADG4UWCA
LGA
OMIT_TABLE
SSD0_OCARINA_LPB_L
SSD_BFH
SSD0_S4E_BOOT2
SSD0_S4E2_SWD_UID0
SSD0_S4E_UART_RX
SSD0_S4E2_SWD_UID1
SSD0_S4E2_UART_TX
SSD0_OCARINA_PFN
SSD0_PCIE_RESET_L
SSD0_SWDIO_UART_D2R
SSD0_SWCLK_UART_R2D
SSD0_S4E2_JTAG_TDO
SSD0_S4E1_JTAG_TDO
SSD0_S4E_JTAG_SEL
SSD0_S4E2_DROOP_L
SSD0_OCARINA_WP_L
EXT_D0/BOOT0
EXT_D1/BOOT1
EXT_D2/BOOT2/SPINAND_SCLK
EXT_D3/SWD_UID0/SPINAND_MISO
EXT_D4/UART_RX
EXT_D5/SWD_UID1/SPINAND_MOSI
EXT_D6/UART_TX
EXT_D7/SPF
EXT_NCE/PERST*
EXT_NRE/JTAG_TMS
EXT_NWE/JTAG_TCK
EXT_RNB/JTAG_TDO
EXT_CLE/JTAG_TDI
EXT_ALE/JTAG_SEL
DROOP_N
WP_N
PLACE_NEAR=U8800.M3:3MM
R8840
100
SSD0_CLK24M_23
SSD0_CLK24M
CLK_IN
PCIE_REFCLK_P
PCIE_REFCLK_M
PCIE_CLKREQ_N
PCI_RESREF
PCIE_RX0_P
PCIE_RX0_M
PCIE_TX0_P
PCIE_TX0_M
PCIE_CLK100M_SSD0_23_P
PCIE_CLK100M_SSD0_23_N
SSD0_CLKREQ2_L
SSD0_S4E2_PCIE_RESREF
PCIE_SSD0_R2D_P<2>
PCIE_SSD0_R2D_N<2>
PCIE_SSD0_R2D_C_P<2>
PCIE_SSD0_R2D_C_N<2>
PCIE_SSD0_D2R_C_P<2>
PCIE_SSD0_D2R_C_N<2>
PCIE_SSD0_D2R_P<2>
PCIE_SSD0_D2R_N<2>
C8803 0.22UF
C8804 0.22UF
C8801 0.22UF
C8802 0.22UF
R8804
3.01K
RESET*
TRST*
ZQ_C
ZQ_L
SSD0_OCARINA_RESET_L
SSD0_S4E_JTAG_TRST_L
SSD0_S4E2_ZQ_C
SSD0_S4E2_ZQ_L
R8805
300
R8806
100
VSS
R8802
47K
R8809
100K
SSD0_S4E2_SWD_UID1
SSD0_S4E2_DROOP_L
SSD0_S4E2_SWD_UID0
R8808
100K
S4E VDD
PP0V9_SSD0
C8810
10UF
C8811
2.2UF
C8812
2.2UF
C8813
0.1UF
C8814
0.1UF
C8815
0.1UF
S4E VDDIO
PP1V8_SSD0
C8832
10UF
C8836
4.3UF
C8837
2.2UF
XW8800
PP1V8_SSD0
PP1V8_SSD0_S4E2_PCI_AVDD_H
VOLTAGE=1.8V
C8844
1.0UF
C8845
0.1UF
XW8801
PP1V8_SSD0_S4E2_AVDD18_PLL
VOLTAGE=1.8V
C8846
1.0UF
C8847
0.1UF
VCC CAP
PP2V7_NAND_SSD0
C8848
10UF
C8849
2.2UF
C8850
2.2UF
BOM_COST_GROUP=SSD
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
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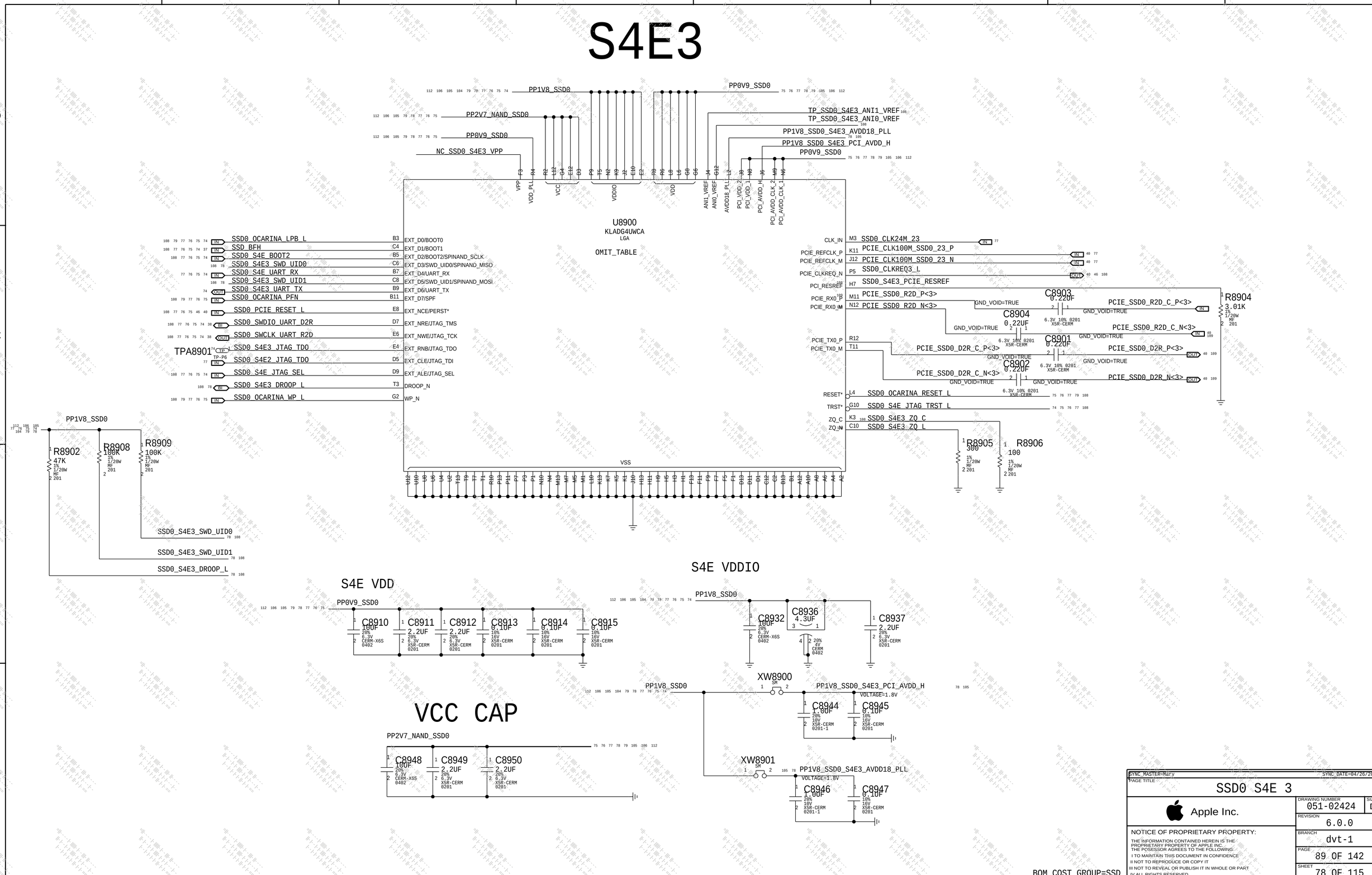
PP1V8_SSD0
PP0V9_SSD0
PP2V7_NAND_SSD0
PP0V9_SSD0
NC_SSD0_S4E3_VPP
TP_SSD0_S4E3_ANI1_VREF
TP_SSD0_S4E3_ANI0_VREF
PP1V8_SSD0_S4E3_AVDD18_PLL
PP1V8_SSD0_S4E3_PCI_AVDD_H
PP0V9_SSD0
VPP
VDD_PLL
VCC
VDDIO
VDD
ANIL_VREF
ANIO_VREF
AVDD18_PLL
PCI_VDD_2
PCI_VDD_1
PCI_AVDD_H
PCI_AVDD_CLK_2
PCI_AVDD_CLK_1
U8900
KLADG4UWCA
LGA
OMIT_TABLE
SSD0_OCARINA_LPB_L
SSD_BFH
SSD0_S4E_BOOT2
SSD0_S4E3_SWD_UID0
SSD0_S4E_UART_RX
SSD0_S4E3_SWD_UID1
SSD0_S4E3_UART_TX
SSD0_OCARINA_PFN
SSD0_PCIE_RESET_L
SSD0_SWDIO_UART_D2R
SSD0_SWCLK_UART_R2D
SSD0_S4E3_JTAG_TDO
SSD0_S4E2_JTAG_TDO
SSD0_S4E_JTAG_SEL
SSD0_S4E3_DROOP_L
SSD0_OCARINA_WP_L
TPA8901
EXT_D0/BOOT0
EXT_D1/BOOT1
EXT_D2/BOOT2/SPINAND_SCLK
EXT_D3/SWD_UID0/SPINAND_MISO
EXT_D4/UART_RX
EXT_D5/SWD_UID1/SPINAND_MOSI
EXT_D6/UART_TX
EXT_D7/SPF
EXT_NCE/PERST*
EXT_NRE/JTAG_TMS
EXT_NWE/JTAG_TCK
EXT_RNB/JTAG_TDO
EXT_CLE/JTAG_TDI
EXT_ALE/JTAG_SEL
DROOP_N
WP_N
CLK_IN
PCIE_REFCLK_P
PCIE_REFCLK_M
PCIE_CLKREQ_N
PCI_RESREF
PCIE_RX0_P
PCIE_RX0_M
PCIE_TX0_P
PCIE_TX0_M
RESET*
TRST*
ZQ_C
ZQ_N
SSD0_CLK24M_23
PCIE_CLK100M_SSD0_23_P
PCIE_CLK100M_SSD0_23_N
SSD0_CLKREQ3_L
SSD0_S4E3_PCIE_RESREF
PCIE_SSD0_R2D_P<3>
PCIE_SSD0_R2D_N<3>
PCIE_SSD0_R2D_C_P<3>
PCIE_SSD0_R2D_C_N<3>
PCIE_SSD0_D2R_C_P<3>
PCIE_SSD0_D2R_C_N<3>
PCIE_SSD0_D2R_P<3>
PCIE_SSD0_D2R_N<3>
SSD0_OCARINA_RESET_L
SSD0_S4E_JTAG_TRST_L
SSD0_S4E3_ZQ_C
SSD0_S4E3_ZQ_L
R8904
3.01K
C8903
C8904
C8901
C8902
R8905
300
R8906
100
R8902
47K
R8908
100K
R8909
100K
SSD0_S4E3_SWD_UID0
SSD0_S4E3_SWD_UID1
SSD0_S4E3_DROOP_L
S4E VDD
PP0V9_SSD0
C8910
C8911
C8912
C8913
C8914
C8915
S4E VDDIO
PP1V8_SSD0
C8932
C8936
4.3UF
C8937
2.2UF
XW8900
PP1V8_SSD0_S4E3_PCI_AVDD_H
VOLTAGE=1.8V
C8944
C8945
XW8901
PP1V8_SSD0_S4E3_AVDD18_PLL
VOLTAGE=1.8V
C8946
C8947
VCC CAP
PP2V7_NAND_SSD0
C8948
C8949
C8950
VSS
BOM_COST_GROUP=SSD
SYNC_MASTER=Mary
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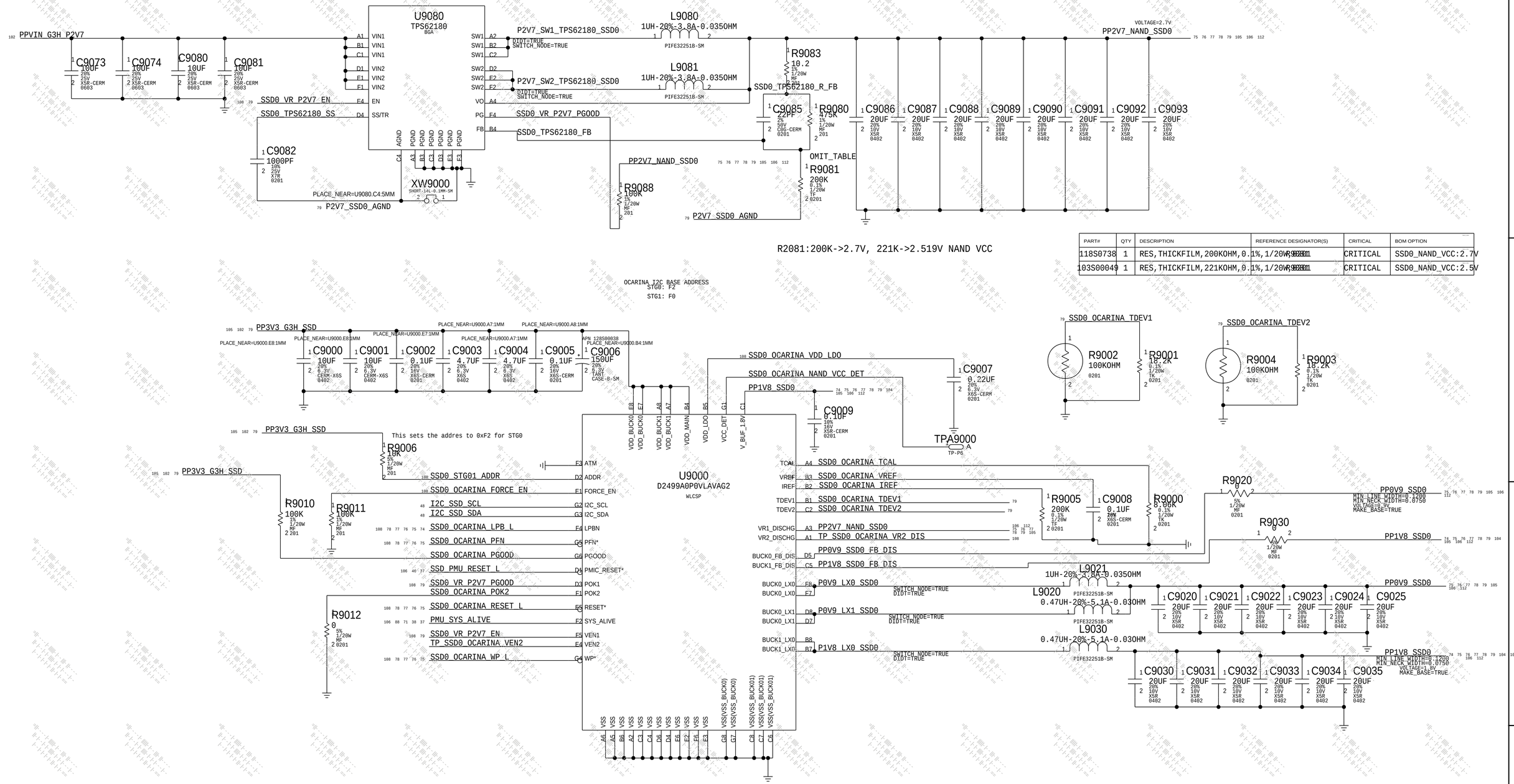

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0738	1	RES,THICKFILM,200KOHM,0.1%,1/20W,0402	R9080	CRITICAL	SSD0_NAND_VCC:2.7V
103S00049	1	RES,THICKFILM,221KOHM,0.1%,1/20W,0402	R9080	CRITICAL	SSD0_NAND_VCC:2.5V

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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SSD0 PMIC & VR

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

ENET:1G CRITICAL L9300 FERR-600-OHM-300MA-0.850OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C9300 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET:1G CRITICAL L9305 FERR-600-OHM-300MA-0.850OHM 0402
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C9305 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET:1G CRITICAL L9310 FERR-600-OHM-300MA-0.850OHM 0402
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R9310 4.7K 5% 1/16W MF-LF 402 ENET:1G
C9310 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9311 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT
ENET_XTALVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

ENET_SR_LX
PP1V2_ENET_INTREG
Internal 1.2V Switching Regulator pins.

PP1V2_ENET_INTREG
396mA (1000base-T, Caesar II)

ENET:1G CRITICAL L9320 FERR-600-OHM-300MA-0.850OHM 0402
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C9321 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9320 4.7UF 20% 6.3V X6S-CERM1 402 ENET:1G

ENET:1G CRITICAL L9325 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C9326 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9325 4.7UF 20% 6.3V X6S-CERM1 402 ENET:1G

ENET:1G CRITICAL L9330 FERR-600-OHM-300MA-0.850OHM 0402
PP1V2_ENET_PHY_GHYPLL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C9331 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9330 4.7UF 20% 6.3V X6S-CERM1 402 ENET:1G

C9336 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9335 10UF 20% 6.3V X5R 603 ENET:1G

PM_SLP_S3_L
R9340 4.7K 5% 1/16W MF-LF 402 ENET:1G
R9341 4.7K 5% 1/16W MF-LF 402 ENET:1G
R9342 1K 5% 1/16W MF-LF 402 ENET:1G
Current Limiting Resistor

C9315 4.7UF 20% 6.3V X5R-CERM 402 ENET:1G
C9316 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

AVDDH, BIASVDDH, XTALVDDH, VDDC, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

OMIT_TABLE
U9300
BCM57766A1KMLG
QFN-8X8
CAESAR IV

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V MAKE_BASE=TRUE
C9380 4.7UF 20% 6.3V X6S-CERM1 402 ENET:1G
C9381 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9382 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET VMAIN PRSNT	58	VMAIN_PRSNT	(IPD-ENET)
PCIE ENET 1G D2R C N	27	PCIE_TXD_N	
PCIE ENET 1G D2R C P	28	PCIE_TXD_P	
PCIE ENET 1G R2D P	33	PCIE_RXD_P	
PCIE ENET 1G R2D N	34	PCIE_RXD_N	
PCIE CLK100M ENET 1G P	31	PCIE_REFCLK_P	
PCIE CLK100M ENET 1G N	30	PCIE_REFCLK_N	
ENET RESET 3V3 L	11	PERST*	(IPD)
ENET_CLKREQ_3V3_L	12	CLKREQ*	(OD)
PCIEDN_WAKE_ENET_L (See note)	3	WAKE*	(OD)
ENET 1G LOW PWR	4	LOW_PWR	(IPD)
SMB ENET SCL	6	SMB_CLK	
SMB ENET SDA	10	SMB_DATA	(IPD-ENETM)
ENET 1G SCLK	66	SCLK_SPD1000LED*	(IPU)
ENET 1G MISO	64	SI/EEDATA	(IPU)
ENET 1G MOSI	65	SO_LINKLED*	(IPU)
ENET 1G CS L	63	CS*/EECLK	(IPU)
TP ENET 1G SERIAL DO	2	SPD100LED*/SERIAL_DO	(OD)
ENET TRAFFICLED L	67	TRAFFICLED*/SERIAL_DI	(OD)
ENET_XTAL_IN	18	XTALI	
ENET_XTAL_OUT	19	XTALO	
ENET_RDAC	38	RDAC	
	69	THRM_PAD	(NO IPU OR IPD-ENET)

TRD0_P	40	ENETCONN_MDI_P<0>	BI
TRD0_N	41	ENETCONN_MDI_N<0>	BI
TRD1_P	44	ENETCONN_MDI_P<1>	BI
TRD1_N	43	ENETCONN_MDI_N<1>	BI
TRD2_P	46	ENETCONN_MDI_P<2>	BI
TRD2_N	47	ENETCONN_MDI_N<2>	BI
TRD3_P	50	ENETCONN_MDI_P<3>	BI
TRD3_N	49	ENETCONN_MDI_N<3>	BI

GPIO_0/CR_ACT_LED*	5	NC	(IPD)
GPIO_1/LR_OUT	8	NC	(IPD)
GPIO_2/MEDIA_SENSE	9	ENET_1G_MEDIA_SENSE	(IPD)
SD_DETECT	1	NC	(IPx-ENET)
CR_CMD	26	NC	(IPU-ENET)
CR_CLK	21	NC	
CR_DATA0	25	NC	(IPU-ENET)
CR_DATA1	24	NC	
CR_DATA2	23	NC	
CR_DATA3	22	NC	
CR_DATA4	52	NC	
CR_DATA5	53	NC	
CR_DATA6	54	NC	
CR_DATA7	55	NC	
MS_INS*	59	NC	(IPU-ENET)
CR_LED*/CR_BUS_PWR	60	NC	(IPU-ENET)
CR_WP*	57	NC	(IPU-ENET)
SR_DISABLE	68	ENET_SR_DISABLE (See note)	

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

CONTROL SIGNAL TO LIGHT LED OR CONTROL SD BUS POWER.

R9381 1K 5% 1/16W MF-LF 402 ENET:1G

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

ENET:1G R9365 1.24K 1% 1/16W MF-LF 402

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L TO PCIEDN_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

PP3V3_ENET

ENET:1G C9390 0.1UF 10% 16V X5R-CERM 0201

U9390 AT45DB011D SOIC-8S1 OMIT_TABLE

ENET_1G_SCLK	2	SCK	
ENET_1G_CS_L	4	CS*	
	5	WP*	
	3	RESET*	
ENET_1G_MOSI	1	SI	
ENET_1G_MISO	8	SO	
	6	VCC	
	7	GND	

NOSTUFF R9390 4.7K 5% 1/16W MF-LF 402
ENET:1G R9397 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

ENET:1G C9340 15PF 2% 50V C0G-CERM 0402
ENET:1G C9341 15PF 2% 50V C0G-CERM 0402
ENET:1G CRITICAL Y9340 25.000MHZ-20PPM-12PF-85C 3.2X2.5MM-SM
NC NC
ENET_XTAL_OUT_R
ENET:1G R9343 0 5% 1/16W MF-LF 402
ENET_XTAL_OUT
NOSTUFF R9344 1M 5% 1/16W MF-LF 402
ENET_XTAL_IN
NOTE: 30 PPM crystal required

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	1G ENET PHY (Caesar IV)
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
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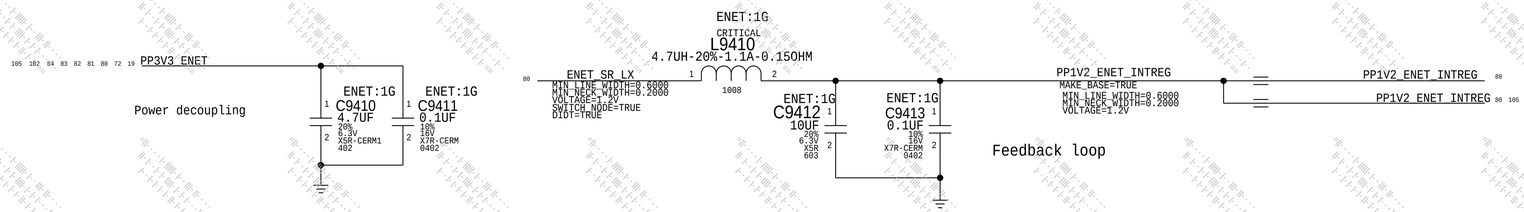
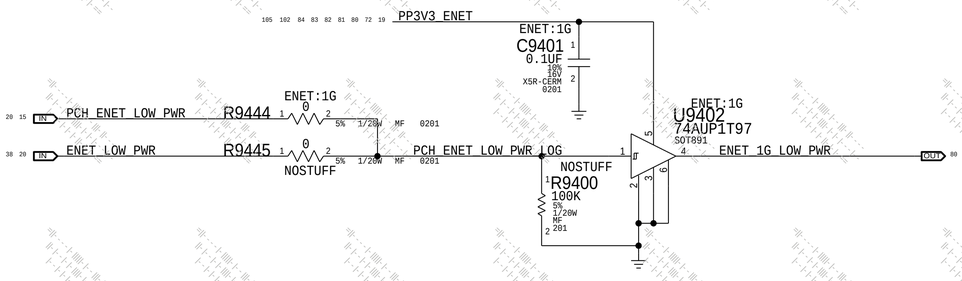
CAESAR IV 1.2V INT.VR CMPTS

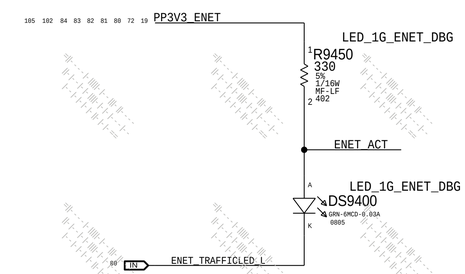


Misc Alias

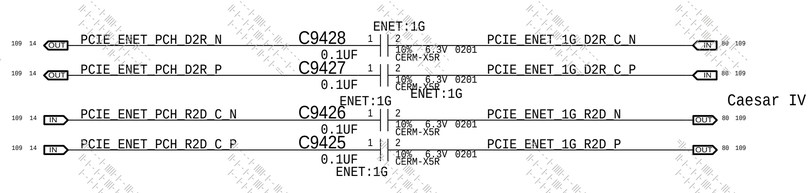
1G ENET LOW PWR



1G ETHERNET ACTIVITY LED



PCIE Connection



BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
1G ENET SUPPORT

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

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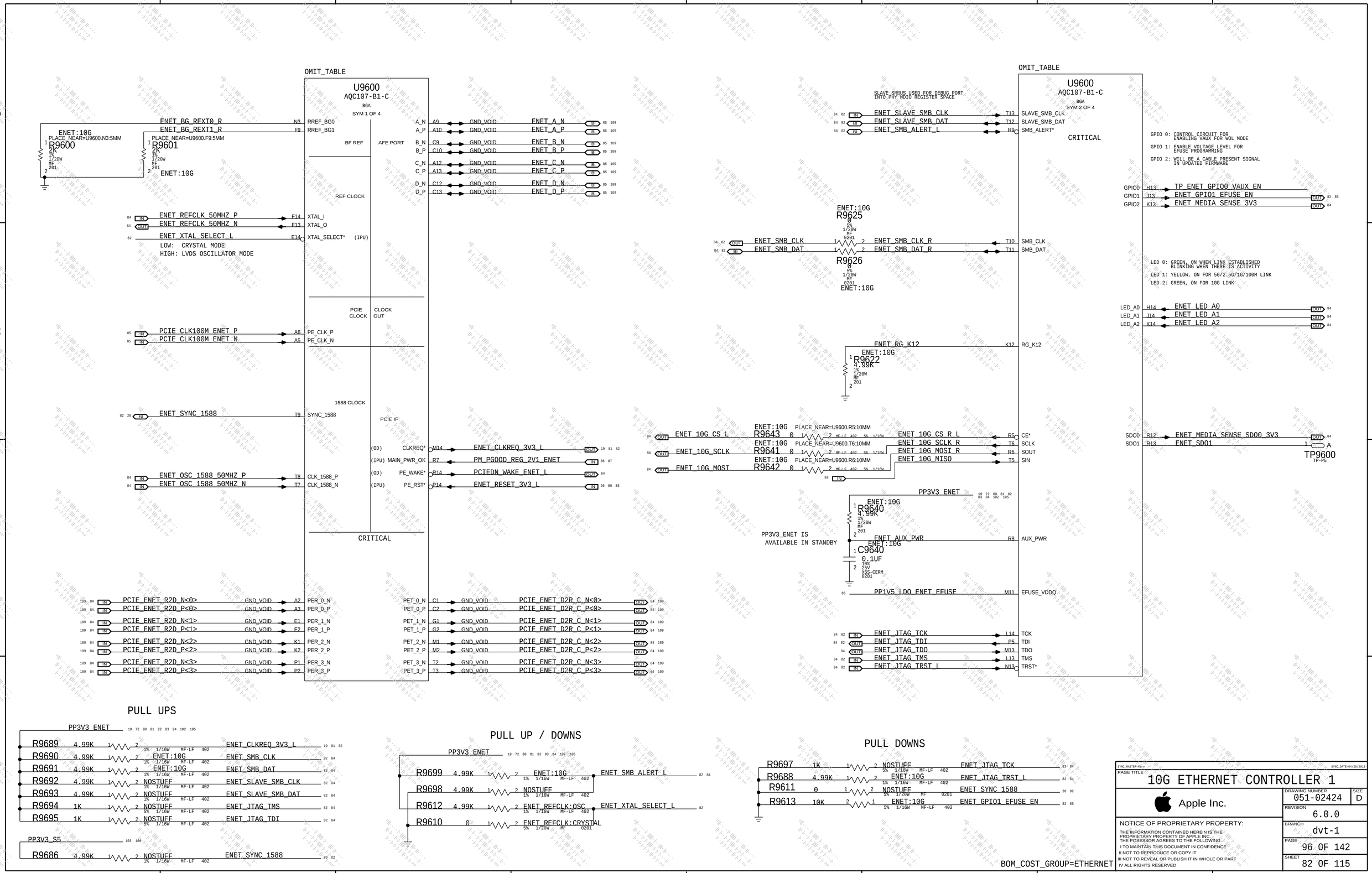
OMIT_TABLE
U9600
AQC107-B1-C
BGA
SYM 1 OF 4
ENET:10G
PLACE_NEAR=U9600.N3:5MM
R9600
2K
1%
1/20W
MF
201
PLACE_NEAR=U9600.F9:5MM
R9601
2K
1%
1/20W
MF
201
ENET:10G
ENET_BG_REXT0_R
ENET_BG_REXT1_R
RREF_BG0
RREF_BG1
BF REF
AFE PORT
A_N A9 GND_VOID ENET_A_N
A_P A10 GND_VOID ENET_A_P
B_N C9 GND_VOID ENET_B_N
B_P C10 GND_VOID ENET_B_P
C_N A12 GND_VOID ENET_C_N
C_P A13 GND_VOID ENET_C_P
D_N C12 GND_VOID ENET_D_N
D_P C13 GND_VOID ENET_D_P
REF CLOCK
ENET_REFCLK_50MHZ_P F14 XTAL_I
ENET_REFCLK_50MHZ_N F13 XTAL_O
ENET_XTAL_SELECT_L E14 XTAL_SELECT* (IPU)
LOW: CRYSTAL MODE
HIGH: LVDS OSCILLATOR MODE
PCIE CLOCK
CLOCK OUT
PCIE_CLK100M_ENET_P A6 PE_CLK_P
PCIE_CLK100M_ENET_N A5 PE_CLK_N
1588 CLOCK
ENET_SYNC_1588 T9 SYNC_1588
PCIE IF
(OD) CLKREQ* M14 ENET_CLKREQ_3V3_L
(IPU) MAIN_PWR_OK R7 PM_PGOOD_REG_2V1_ENET
(OD) PE_WAKE* R14 PCIEDN_WAKE_ENET_L
(IPU) PE_RST* P14 ENET_RESET_3V3_L
ENET_OSC_1588_50MHZ_P T8 CLK_1588_P
ENET_OSC_1588_50MHZ_N T7 CLK_1588_N
CRITICAL
PCIE_ENET_R2D_N<0> GND_VOID A2 PER_0_N
PCIE_ENET_R2D_P<0> GND_VOID A3 PER_0_P
PCIE_ENET_R2D_N<1> GND_VOID E1 PER_1_N
PCIE_ENET_R2D_P<1> GND_VOID E2 PER_1_P
PCIE_ENET_R2D_N<2> GND_VOID K1 PER_2_N
PCIE_ENET_R2D_P<2> GND_VOID K2 PER_2_P
PCIE_ENET_R2D_N<3> GND_VOID P1 PER_3_N
PCIE_ENET_R2D_P<3> GND_VOID P2 PER_3_P
PET_0_N C1 GND_VOID PCIE_ENET_D2R_C_N<0>
PET_0_P C2 GND_VOID PCIE_ENET_D2R_C_P<0>
PET_1_N G1 GND_VOID PCIE_ENET_D2R_C_N<1>
PET_1_P G2 GND_VOID PCIE_ENET_D2R_C_P<1>
PET_2_N M1 GND_VOID PCIE_ENET_D2R_C_N<2>
PET_2_P M2 GND_VOID PCIE_ENET_D2R_C_P<2>
PET_3_N T2 GND_VOID PCIE_ENET_D2R_C_N<3>
PET_3_P T3 GND_VOID PCIE_ENET_D2R_C_P<3>
OMIT_TABLE
U9600
AQC107-B1-C
BGA
SYM 2 OF 4
SLAVE SMBUS USED FOR DEBUG PORT
INTO PHY MDIO REGISTER SPACE
ENET_SLAVE_SMB_CLK T13 SLAVE_SMB_CLK
ENET_SLAVE_SMB_DAT T12 SLAVE_SMB_DAT
ENET_SMB_ALERT_L R9 SMB_ALERT*
CRITICAL
GPIO 0: CONTROL CIRCUIT FOR
ENABLING VAUX FOR WOL MODE
GPIO 1: ENABLE VOLTAGE LEVEL FOR
EFUSE PROGRAMMING
GPIO 2: WILL BE A CABLE PRESENT SIGNAL
IN UPDATED FIRMWARE
GPIO0 H13 TP_ENET_GPIO0_VAUX_EN
GPIO1 J13 ENET_GPIO1_EFUSE_EN
GPIO2 K13 ENET_MEDIA_SENSE_3V3
ENET:10G
R9625
0
5%
1/20W
MF
0201
ENET:10G
R9626
0
5%
1/20W
MF
0201
ENET:10G
ENET_SMB_CLK ENET_SMB_CLK_R T10 SMB_CLK
ENET_SMB_DAT ENET_SMB_DAT_R T11 SMB_DAT
LED 0: GREEN, ON WHEN LINK ESTABLISHED
BLINKING WHEN THERE IS ACTIVITY
LED 1: YELLOW, ON FOR 5G/2.5G/1G/100M LINK
LED 2: GREEN, ON FOR 10G LINK
LED_A0 H14 ENET_LED_A0
LED_A1 J14 ENET_LED_A1
LED_A2 K14 ENET_LED_A2
ENET_RG_K12 K12 RG_K12
ENET:10G
R9622
4.99K
1%
1/20W
MF
201
ENET:10G PLACE_NEAR=U9600.R5:10MM
R9643 0 MF-LF 402 5% 1/16W
ENET:10G PLACE_NEAR=U9600.T6:10MM
R9641 0 MF-LF 402 5% 1/16W
ENET:10G PLACE_NEAR=U9600.R6:10MM
R9642 0 MF-LF 402 5% 1/16W
ENET_10G_CS_L
ENET_10G_SCLK
ENET_10G_MOSI
ENET_10G_CS_R_L R5 CE*
ENET_10G_SCLK_R T6 SCLK
ENET_10G_MOSI_R R6 SOUT
ENET_10G_MISO T5 SIN
SDO0 R12 ENET_MEDIA_SENSE_SDO0_3V3
SDO1 R13 ENET_SDO1
TP9600
TP-P5
PP3V3_ENET
ENET:10G
R9640
4.99K
1%
1/20W
MF
201
PP3V3_ENET IS
AVAILABLE IN STANDBY
ENET_AUX_PWR R8 AUX_PWR
ENET:10G
C9640
0.1UF
10%
25V
X6S-CERM
0201
PP1V5_LDO_ENET_EFUSE M11 EFUSE_VDDQ
ENET_JTAG_TCK L14 TCK
ENET_JTAG_TDI P5 TDI
ENET_JTAG_TDO M13 TDO
ENET_JTAG_TMS L13 TMS
ENET_JTAG_TRST_L N13 TRST*
PULL UPS
PP3V3_ENET
R9689 4.99K ENET_CLKREQ_3V3_L
R9690 4.99K ENET:10G ENET_SMB_CLK
R9691 4.99K ENET:10G ENET_SMB_DAT
R9692 4.99K NOSTUFF ENET_SLAVE_SMB_CLK
R9693 4.99K NOSTUFF ENET_SLAVE_SMB_DAT
R9694 1K NOSTUFF ENET_JTAG_TMS
R9695 1K NOSTUFF ENET_JTAG_TDI
PP3V3_S5
R9686 4.99K NOSTUFF ENET_SYNC_1588
PULL UP / DOWNS
PP3V3_ENET
R9699 4.99K ENET:10G ENET_SMB_ALERT_L
R9698 4.99K NOSTUFF
R9612 4.99K ENET_REFCLK:OSC ENET_XTAL_SELECT_L
R9610 0 ENET_REFCLK:CRYSTAL
PULL DOWNS
R9697 1K NOSTUFF ENET_JTAG_TCK
R9688 4.99K ENET:10G ENET_JTAG_TRST_L
R9611 0 NOSTUFF ENET_SYNC_1588
R9613 10K ENET:10G ENET_GPIO1_EFUSE_EN
BOM_COST_GROUP=ETHERNET
SYNC_MASTER=MGrY
SYNC_DATE=04/26/2018
PAGE TITLE
10G ETHERNET CONTROLLER 1
Apple Inc.
DRAWING NUMBER
051-02424
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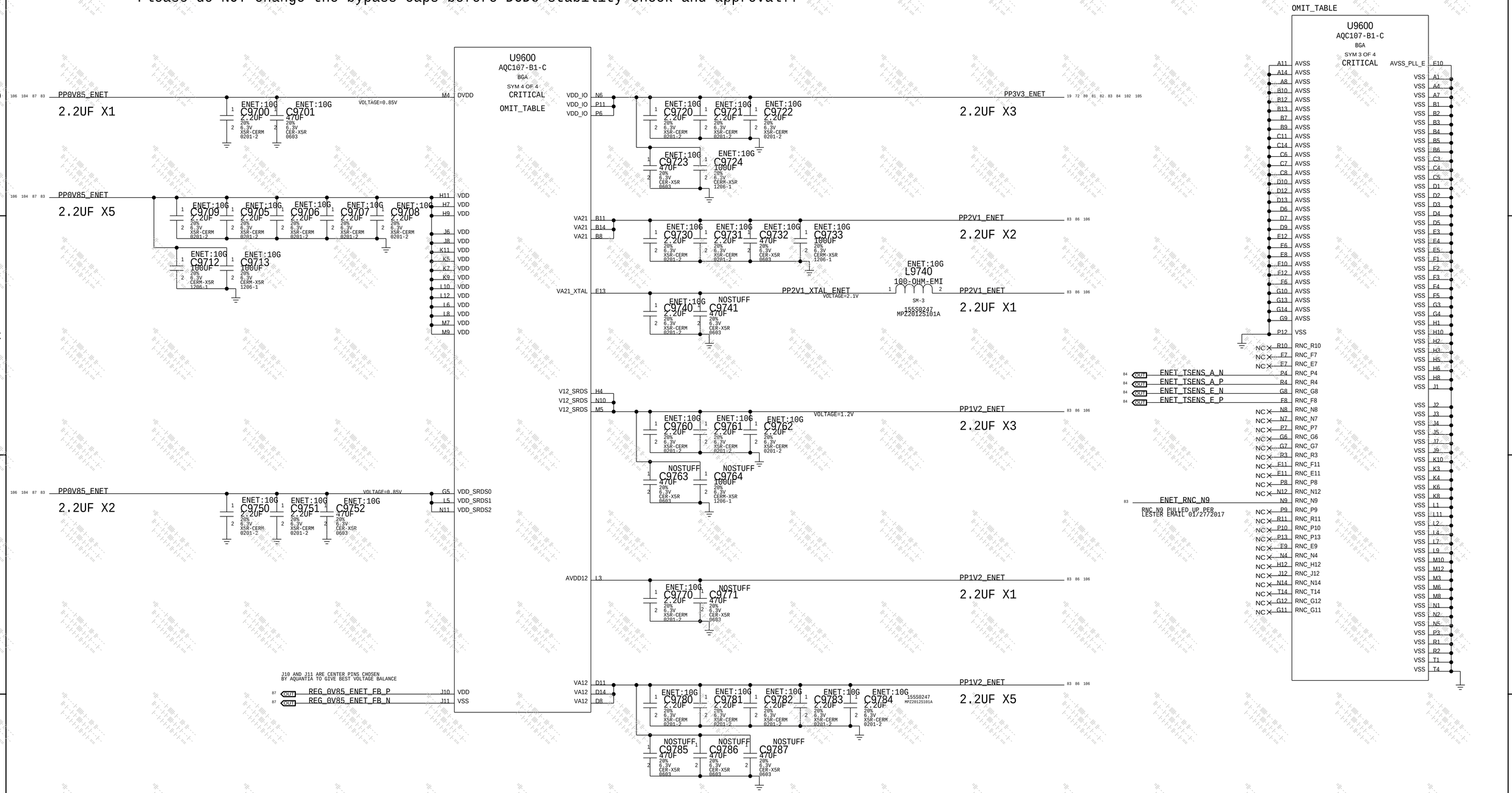
Please do NOT change the bypass caps before DCDC stability check and approval!!



BOM_COST_GROUP=ETHERNET

PAGE TITLE	10G ETHERNET CONTROLLER 2
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R2D ETHERNET PCIE CAPS

PCIE_ENET_R2D_C_N<0> — C9840 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<0>
PCIE_ENET_R2D_C_P<0> — C9841 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<0>
PCIE_ENET_R2D_C_N<1> — C9842 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<1>
PCIE_ENET_R2D_C_P<1> — C9843 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<1>
PCIE_ENET_R2D_C_N<2> — C9844 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<2>
PCIE_ENET_R2D_C_P<2> — C9845 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<2>
PCIE_ENET_R2D_C_N<3> — C9846 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<3>
PCIE_ENET_R2D_C_P<3> — C9847 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<3>

D2R ETHERNET PCIE CAPS

PCIE_ENET_D2R_C_N<0> — C9850 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<0>
PCIE_ENET_D2R_C_P<0> — C9851 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<0>
PCIE_ENET_D2R_C_N<1> — C9852 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<1>
PCIE_ENET_D2R_C_P<1> — C9853 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<1>
PCIE_ENET_D2R_C_N<2> — C9854 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<2>
PCIE_ENET_D2R_C_P<2> — C9855 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<2>
PCIE_ENET_D2R_C_N<3> — C9856 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<3>
PCIE_ENET_D2R_C_P<3> — C9857 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<3>

1588 EXTERNAL LVDS OSCILLATOR

PP3V3_ENET — L9860 FERR-600-OHM-2A 0805 ENET:10G
C9860 2.2UF 20% 6.3V X5R-CERM 0201-2 ENET:10G
R9866 0 5% 1/16W MF-LF 402 ENET:10G
PP3V3_G3H_1588_OSC VOLTAGE=3.3V
C9861 47UF 20% 6.3V CER-X5R 0603 ENET:10G
C9862 0.1UF 10% 6.3V X7R 0201 ENET:10G
U9860 50MHZ-50PPM-3.3V 5.00X3.20-SM ENET:10G
OSC_1588_OE — OE
NC — NC
OUT — OSC_1588_50MHZ_P — R9864 NOSTUFF 0 1/16W 5% MF-LF 402 — ENET_OSC_1588_50MHZ_P
OUT* — OSC_1588_50MHZ_N — R9865 NOSTUFF 0 1/16W 5% MF-LF 402 — ENET_OSC_1588_50MHZ_N
VDD, GND

FLASH MEMORY

ENET:10G R9890 1K 5% 1/16W MF-LF 402
ENET:10G R9891 1K 5% 1/16W MF-LF 402
ENET:10G R9892 4.99K 1% 1/20W MF 201
PP3V3_ENET — ENET:10G C9890 1.00UF 10% 25V X6S 0402
U9890 32MB-85MHZ-2.3V-3.6V SOIC CRITICAL AT45DB321E OMIT_TABLE
VCC, GND
ENET_10G_SCLK — SCK
ENET_10G_CS_L — CS*
ENET_10G_SPI_WP_L — WP*
ENET_10G_SPI_RST_L — RESET*
ENET_10G_MOSI — SI
ENET_10G_MISO_R — SO — R9893 ENET:10G 0 1/16W 5% MF-LF 402 PLACE_NEAR=U9890.8:5MM — ENET_10G_MISO

JTAG TPS

ENET_JTAG_TRST_L — TP9820
ENET_JTAG_TDI — TP9821
ENET_JTAG_TCK — TP9822
ENET_JTAG_TMS — TP9823
ENET_JTAG_TDO — TP9824

ETHERNET ACTIVITY LEDS

PP3V3_ENET
DEBUG_LEDS:10G R9830 390 5% 1/16W MF-LF 402 — ENET0_LED — DEBUG_LEDS:10G DS9830 GRN-0MCD-0.03A 0805
DEBUG_LEDS:10G R9831 390 5% 1/16W MF-LF 402 — ENET1_LED — DEBUG_LEDS:10G DS9831 AMBER-605NM-35-56MCD LTST-C281KFKT-5M
DEBUG_LEDS:10G R9832 390 5% 1/16W MF-LF 402 — ENET2_LED — DEBUG_LEDS:10G DS9832 GRN-0MCD-0.03A 0805
ENET_LED_A0
ENET_LED_A1
ENET_LED_A2

AQC ON-DIE THERMAL SENSE (TIED)

ENET_TSENS_A_N — R9860 NOSTUFF 0 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1
ENET_TSENS_E_N — R9861 ENET:10G 0 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1 — ENET_TSENS_N
ENET_TSENS_A_P — R9862 NOSTUFF 0 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1
ENET_TSENS_E_P — R9863 ENET:10G 0 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1 — ENET_TSENS_P

SPARE MOSFET

NC_MEDIA_SENSE_SF_G
NC_MEDIA_SENSE_SF_S
NC_MEDIA_SENSE_SF_D
Q9880 DMN5L06VK-7 VTH MAX IS 1.0 V VER 5 SOT563

ENET WAKE LEVEL SHIFTER

PP3V3_ENET — R9820 47K 5% 1/20W MF 201 — PCIEDN_WAKE
R9821 47K 5% 1/20W MF 201
MAKE_BASE=TRUE
PCIEDN_WAKE_ENET_L — Q9820 DMN5L06VK-7 SOT563 VER 4 VTH MAX IS 1.0 V — PCIEDN_WAKE_ENET_L
PP1V8_SLPS2R — NOSTUFF R9822 47K 5% 1/20W MF 201 — PCIEDN_WAKE_L
ENET_WAKE_HAS_IPU
Q9820 DMN5L06VK-7 SOT563 VER 4 VTH MAX IS 1.0 V

50 MHZ REFCLK OSCILLATOR

PP3V3_ENET — L9880 FERR-600-OHM-2A 0805 ENET:10G
C9880 2.2UF 20% 6.3V X5R-CERM 0201 ENET:10G
R9889 0 5% 1/10W MF-LF 402 ENET:10G
PP3V3_G3H_ENET_REFCLK VOLTAGE=3.3V
C9881 47UF 20% 6.3V CER-X5R 0603 ENET:10G
C9882 0.1UF 10% 6.3V X7R 0201 ENET:10G
U9880 50MHZ-50PPM-3.3V 5.00X3.20-SM ENET:10G
OSC_REFCLK_OE — OE
NC — NC
OUT — ENET_OSC_REFCLK_50MHZ_P
OUT* — ENET_OSC_REFCLK_50MHZ_N
VDD, GND

USE OSCILLATOR BY DEFAULT

ENET_REFCLK:OSC
R9808 0 1/20W 5% MF 0201 PLACE_NEAR=R9806.2:1MM — ENET_REFCLK_50MHZ_P
R9807 0 1/20W 5% MF 0201 PLACE_NEAR=R9805.2:1MM — ENET_REFCLK_50MHZ_N
ENET_REFCLK:CRYSTAL
R9805 0 1/20W 5% MF 0201
R9806 0 1/20W 5% MF 0201
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1

50 MHZ REFCLK CRYSTAL

ENET:10G C9800 3.0PF +/-0.25PF 25V NP0-C0G 0201
ENET_XTALO_R — ENET:10G R9800 0 5% 1/10W MF-LF 402 NO_XNET_CONNECTION=1 — ENET_XTALO
ENET:10G Y9800 50MHZ-45PPM-8PF 2.0X1P6-SM PLACE_NEAR=U9600.F14:5.5MM APN 197S00104
NC, NC
NO_XNET_CONNECTION=1 NOSTUFF R9801 1M 5% 1/10W MF-LF 402
ENET:10G C9801 3.0PF +/-0.25PF 25V NP0-C0G 0201
ENET_XTALI

BOM_COST_GROUP=ETHERNET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	2	dual FET	Q9820,Q1935	CRITICAL	

ENET MEDIA SENSE LEVEL SHIFTER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	1	dual FET	Q9880	CRITICAL	ENET:1G

OMIT_TABLE Q9880 DMN5L06VK-7 SOT563 VER 3 VTH MAX IS 1.0 V
PP1V8_SLPS2R
ENET_MEDIA_SENSE_3V3 — R9887 NOSTUFF 0 1/16W 5% MF-LF 402
ENET_MEDIA_SENSE_SD00_3V3 — R9888 NOSTUFF 0 1/16W 5% MF-LF 402 — ENET_SENSE_FET_LS
From Caesar IV — ENET_1G_MEDIA_SENSE — R9899 ENET:1G 0 1/16W 5% MF-LF 402
R9885 100K 5% 1/20W MF 201
R9886 50K 5% 1/20W MF 201
ENET_MEDIA_SENSE

ETHERNET SLAVE SMBUS DEBUG

ENET_SLAVE_SMB_CLK — TP9800
ENET_SLAVE_SMB_DAT — TP9801
TP9802

ETHERNET MULTI-MASTER SMBUS DEBUG

ENET_SMB_ALERT_L — TP9807
ENET_SMB_CLK — TP9805
ENET_SMB_DAT — TP9806
TP9808

LAYOUT NOTE: PLACE TPS AT 0.1MM PITCH IN STRAIGHT ROW IN SAME ORDER SHOWN HERE

SYNC_MASTER=MGrr SYNC_DATE=04/26/2010

PAGE TITLE: 10G ENET SUPPORT 1

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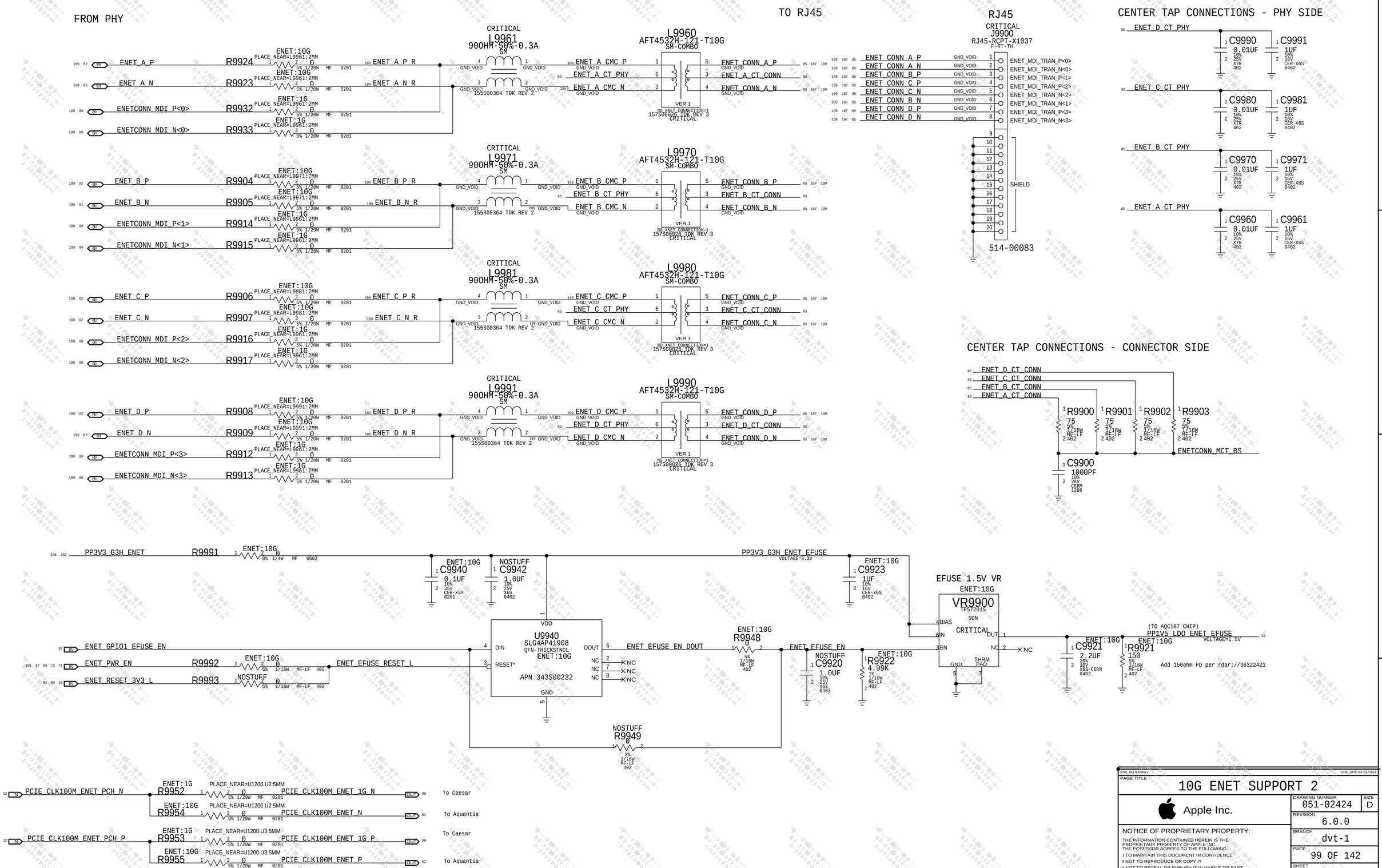
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 98 OF 142
SHEET: 84 OF 115


FROM PHY
TO RJ45
RJ45
CRITICAL
J9900
RJ45-RCPT-X1037
F-RT-TH
CENTER TAP CONNECTIONS - PHY SIDE
CENTER TAP CONNECTIONS - CONNECTOR SIDE
ENET_A_P
ENET_A_N
ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENET_B_P
ENET_B_N
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENET_C_P
ENET_C_N
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENET_D_P
ENET_D_N
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
L9960
L9970
L9980
L9990
AFT4532H-121-T10G
SM-COMBO
155S00364 TDK REV 2
157S00026 TDK REV 3
514-00083
SHIELD
ENET_D_CT_PHY
ENET_C_CT_PHY
ENET_B_CT_PHY
ENET_A_CT_PHY
ENET_D_CT_CONN
ENET_C_CT_CONN
ENET_B_CT_CONN
ENET_A_CT_CONN
ENETCONN_MCT_BS
PP3V3_G3H_ENET
PP3V3_G3H_ENET_EFUSE
EFUSE 1.5V VR
VR9900
TPS72015
SON
U9940
SLG4AP41908
QFN-THICKSTNCL
APN 343S00232
ENET_GPIO1_EFUSE_EN
ENET_PWR_EN
ENET_RESET_3V3_L
ENET_EFUSE_RESET_L
ENET_EFUSE_EN_DOUT
ENET_EFUSE_EN
PP1V5_LDO_ENET_EFUSE
Add 150ohm PD per rdar://36322421
PCIE_CLK100M_ENET_PCH_N
PCIE_CLK100M_ENET_PCH_P
PCIE_CLK100M_ENET_1G_N
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_1G_P
PCIE_CLK100M_ENET_P
To Caesar
To Aquantia
BOM_COST_GROUP=ETHERNET
PAGE TITLE
10G ENET SUPPORT 2
Apple Inc.
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051-02424
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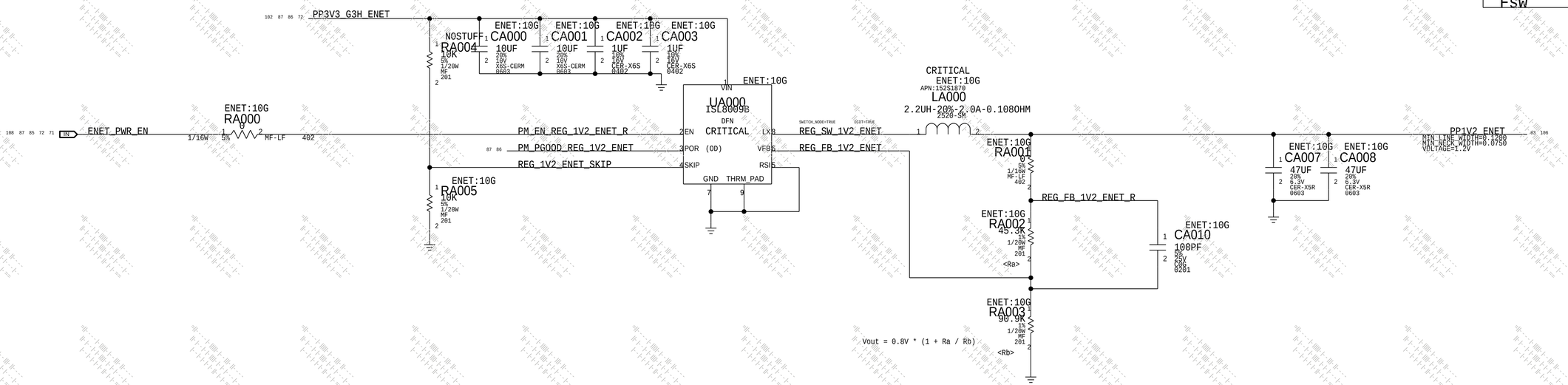
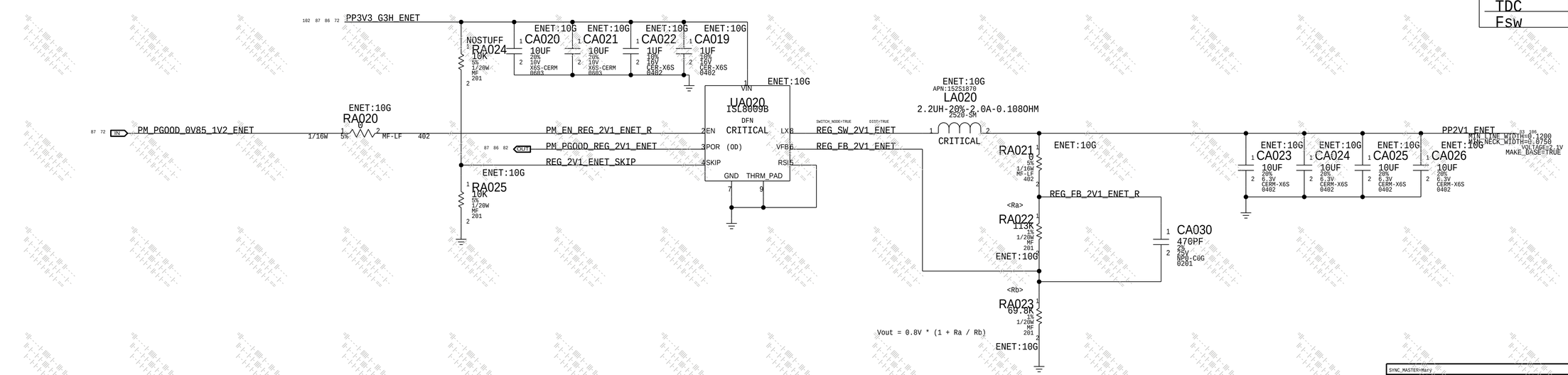
ENET 1V2 REGULATOR	
VOUT	1.20 V
EDC	1 A
OC (TYP)	2.2 A
TDC	0.9 A
Fsw	1.6 MHZ

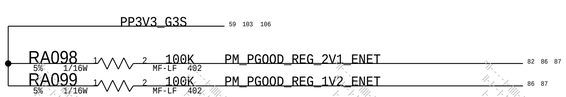
1.2V ENET REGULATOR



ENET 2V1 REGULATOR	
VOUT	2.10 V
EDC	0.5 A
OC (TYP)	2.2 A
TDC	0.4 A
Fsw	1.6 MHZ

2.1V ENET REGULATOR





BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: VR 10G ENET 1V2, 2V1

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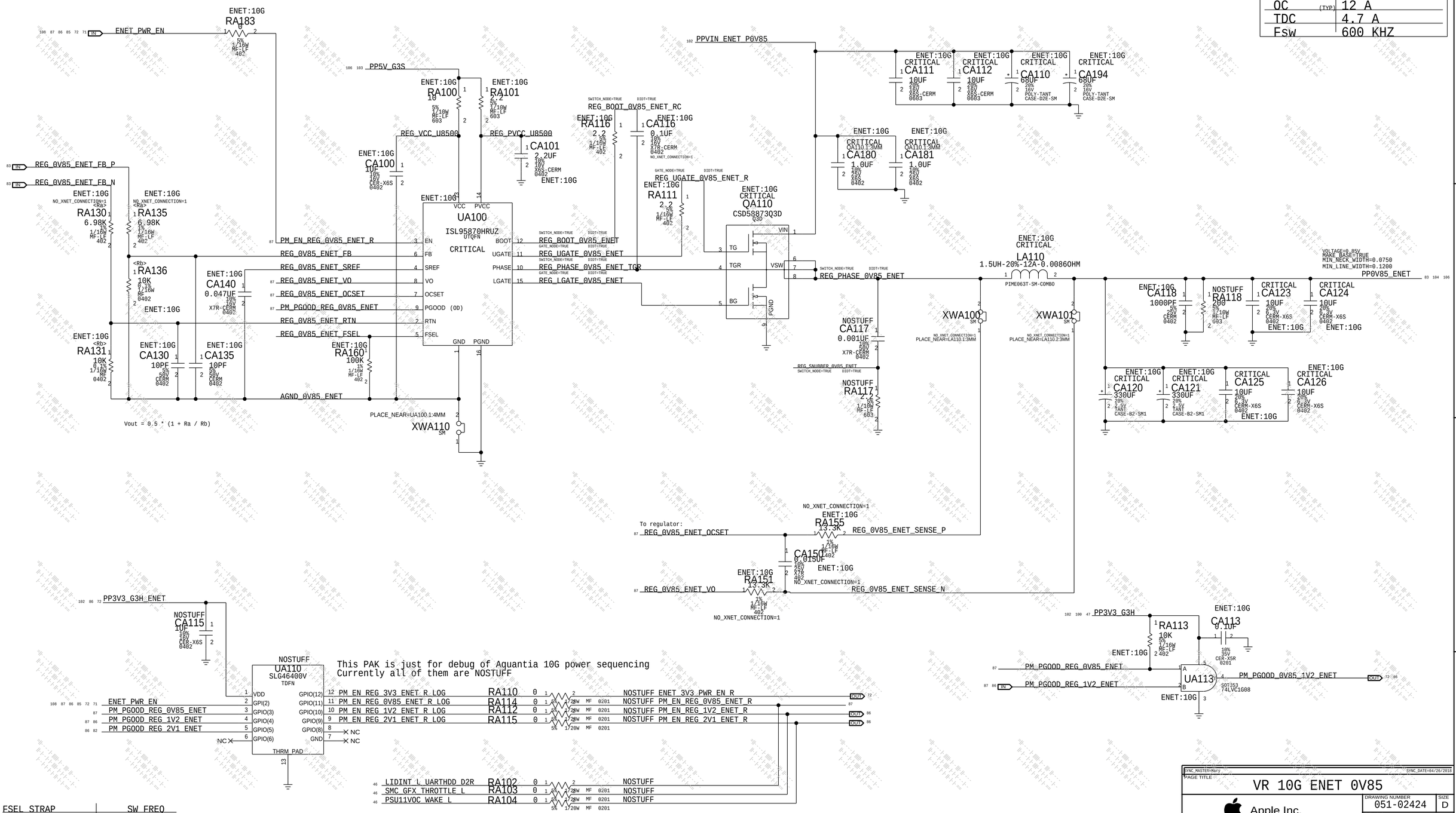
ENET 0V85 REGULATOR	
VOUT	0.85 V
EDC	6.5 A
OC (TYP)	12 A
TDC	4.7 A
Fsw	600 KHZ



This PAK is just for debug of Aquantia 10G power sequencing
Currently all of them are NOSTUFF

ESEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: VR 10G ENET 0V85

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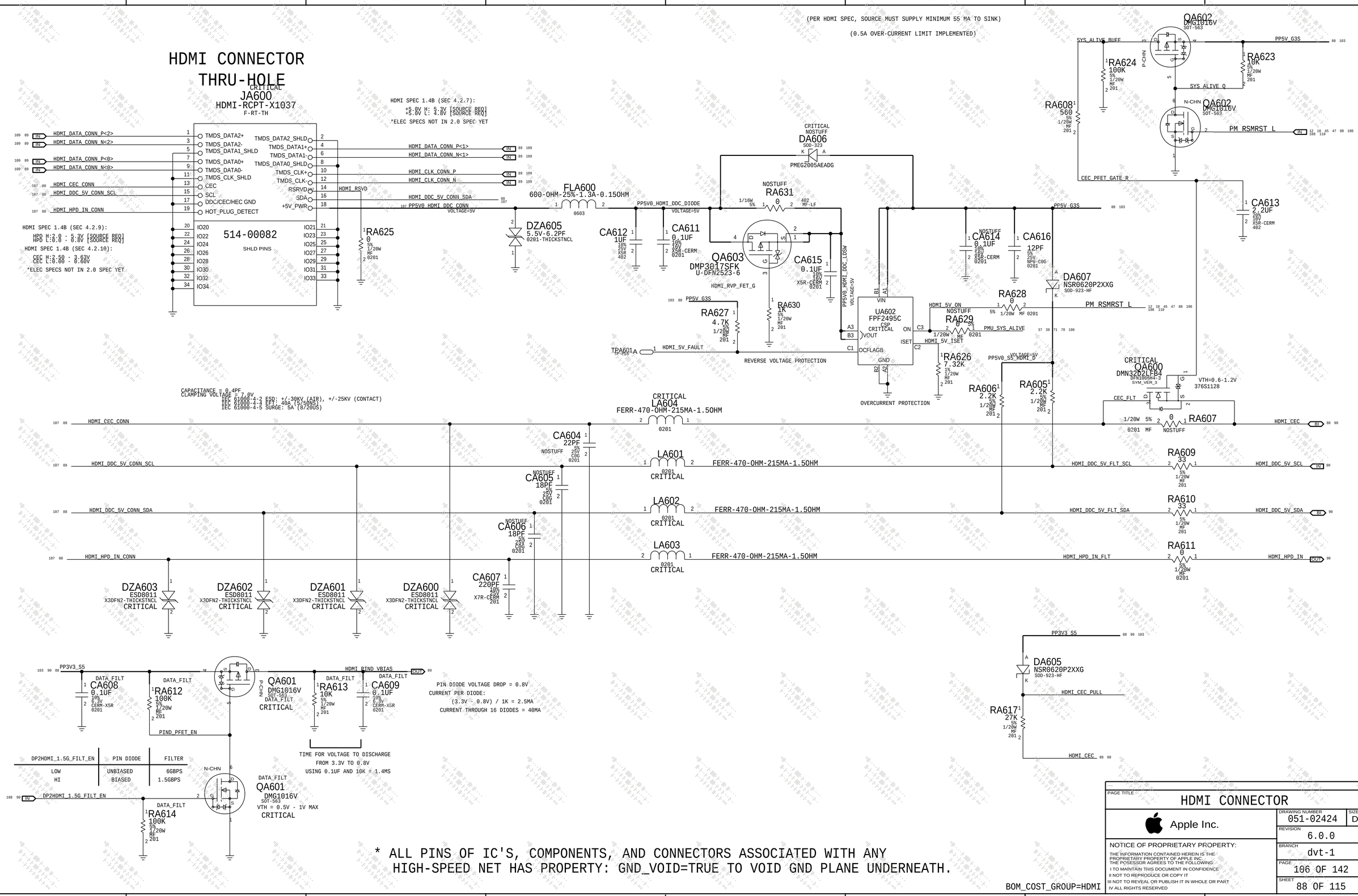
HDMI CONNECTOR
THRU-HOLE
CRITICAL
JA600
HDMI-RCPT-X1037
F-RT-TH
514-00082
SHLD PINS
HDMI SPEC 1.4B (SEC 4.2.7):
+5.0V H: 5.3V [SOURCE REQ]
+5.0V L: 4.8V [SOURCE REQ]
*ELEC SPECS NOT IN 2.0 SPEC YET
HDMI SPEC 1.4B (SEC 4.2.9):
HPD H:3.0 - 5.3V [SOURCE REQ]
HPD L:0.0 - 0.8V [SOURCE REQ]
HDMI SPEC 1.4B (SEC 4.2.10):
CEC H:2.50 - 3.63V
CEC L:0.00 - 0.60V
*ELEC SPECS NOT IN 2.0 SPEC YET
(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)
(0.5A OVER-CURRENT LIMIT IMPLEMENTED)
FLA600
600-OHM-25%-1.3A-0.150HM
DZA605
5.5V-6.2PF
0201-THICKSTNCL
CA612
1UF
CA611
0.1UF
OA603
DMP3017SFK
U-DFN2523-6
HDMI_RVP_FET_G
CA615
0.1UF
RA627
4.7K
RA630
1K
TPA601A
HDMI_5V_FAULT
REVERSE VOLTAGE PROTECTION
DA606
PMEG2005AEADG
RA631
UA602
FPF2495C
CSP
CRITICAL
OVERCURRENT PROTECTION
OA602
DMG1016V
SOT-563
P-CHN
N-CHN
RA624
100K
RA623
10K
RA608
560
PM_RSMRST_L
CA613
2.2UF
CA614
0.1UF
CA616
12PF
DA607
NSR0620P2XXG
SOD-923-HF
RA628
RA629
RA626
7.32K
RA606
2.2K
RA605
2.2K
OA600
DMN32D2LFB4
DFN1006H4-3
VTH=0.6-1.2V
376S1128
RA607
RA609
33
RA610
33
RA611
0
HDMI_CEC
HDMI_DDC_5V_SCL
HDMI_DDC_5V_SDA
HDMI_HPD_IN
LA604
FERR-470-OHM-215MA-1.5OHM
LA601
LA602
LA603
CA604
22PF
CA605
18PF
CA606
18PF
CA607
220PF
DZA603
DZA602
DZA601
DZA600
ESD8011
X3DFN2-THICKSTNCL
CAPACITANCE = 0.4PF
CLAMPING VOLTAGE = 7.0V
IEC 61000-4-2 ESD: +/-30KV (AIR), +/-25KV (CONTACT)
IEC 61000-4-4 EFT: 40A (5/50NS)
IEC 61000-4-5 SURGE: 5A (8/20US)
QA601
DMG1016V
SOT-563
VTH = 0.5V - 1V MAX
CRITICAL
RA612
100K
RA613
10K
CA608
0.1UF
CA609
0.1UF
PIN DIODE VOLTAGE DROP = 0.8V
CURRENT PER DIODE:
(3.3V - 0.8V) / 1K = 2.5MA
CURRENT THROUGH 16 DIODES = 40MA
TIME FOR VOLTAGE TO DISCHARGE
FROM 3.3V TO 0.8V
USING 0.1UF AND 10K = 1.4MS
DP2HDMI_1.5G_FILT_EN
LOW
HI
PIN DIODE
UNBIASED
BIASED
FILTER
6GBPS
1.5GBPS
RA614
100K
DA605
NSR0620P2XXG
SOD-923-HF
RA617
27K
HDMI_CEC_PULL
* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY
HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.
BOM_COST_GROUP=HDMI
PAGE TITLE
HDMI CONNECTOR
Apple Inc.
DRAWING NUMBER
051-02424
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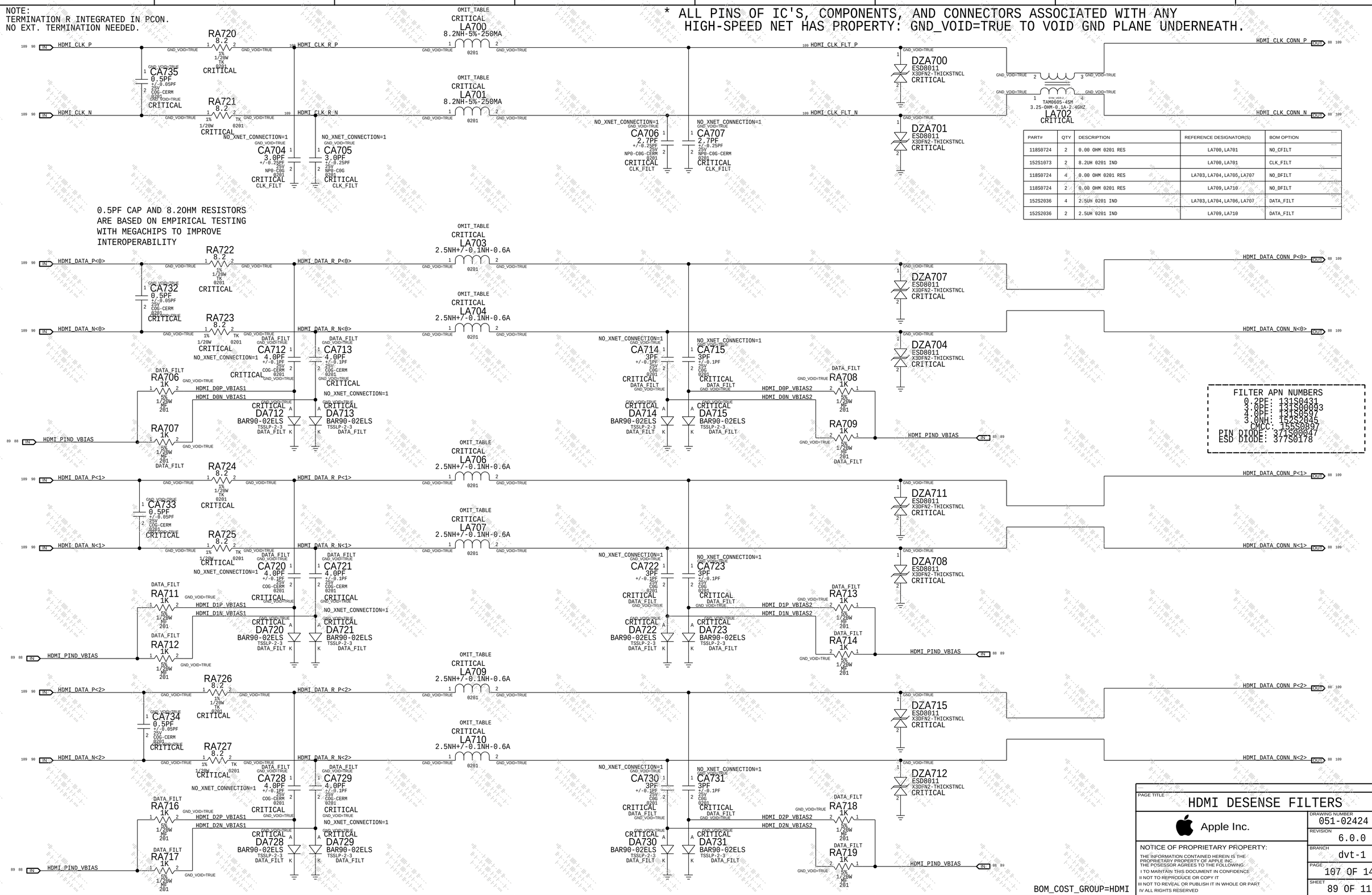
NOTE:
TERMINATION R INTEGRATED IN PCON.
NO EXT. TERMINATION NEEDED.

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0724	2	0.00 OHM 0201 RES	LA700,LA701	NO_CFILT
152S1073	2	8.2UH 0201 IND	LA700,LA701	CLK_FILT
118S0724	4	0.00 OHM 0201 RES	LA703,LA704,LA706,LA707	NO_DFILT
118S0724	2	0.00 OHM 0201 RES	LA709,LA710	NO_DFILT
152S2036	4	2.5UH 0201 IND	LA703,LA704,LA706,LA707	DATA_FILT
152S2036	2	2.5UH 0201 IND	LA709,LA710	DATA_FILT

PAGE TITLE: HDMI DESENSE FILTERS

Apple Inc.

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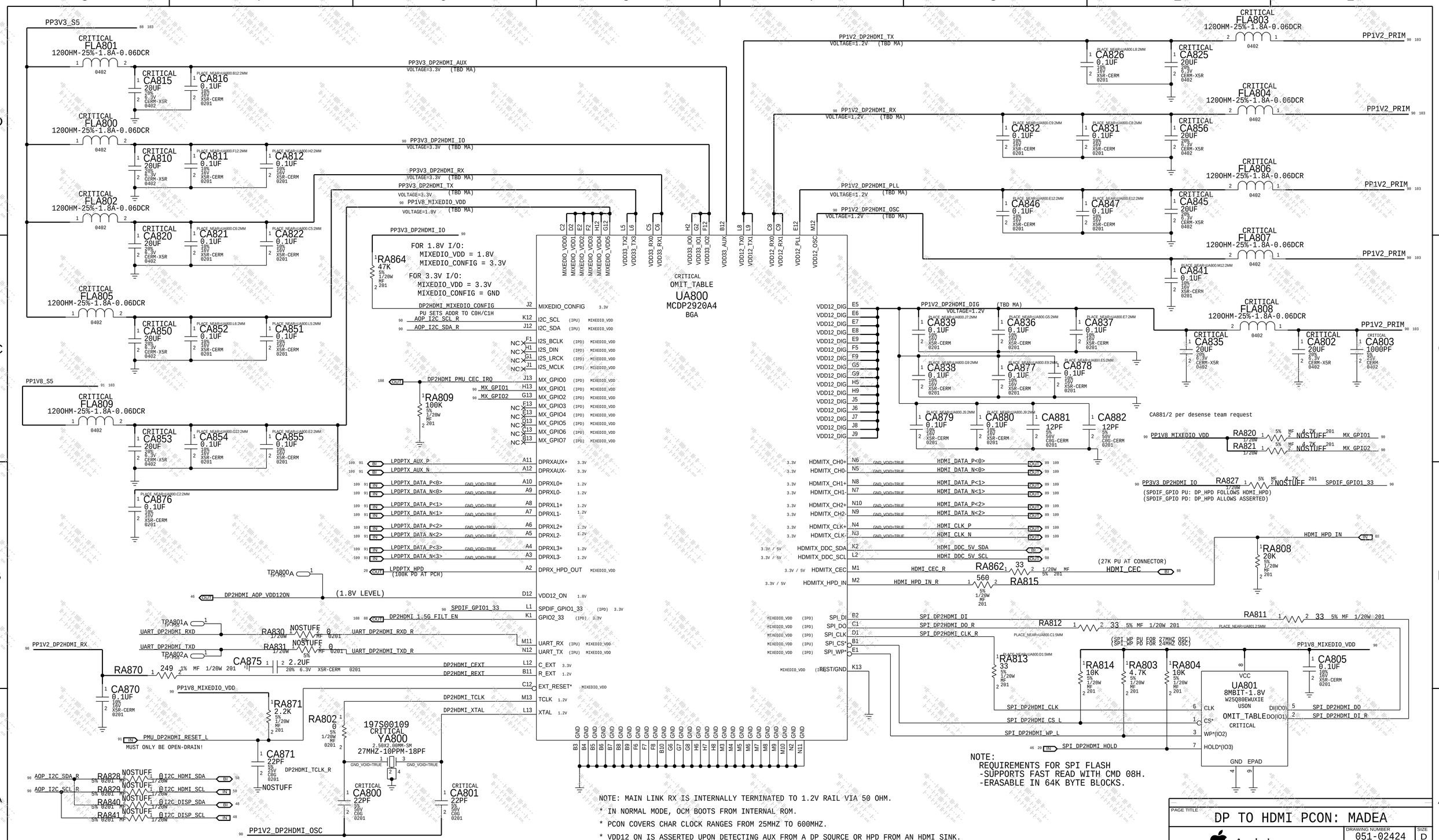

NOTE: MAIN LINK RX IS INTERNALLY TERMINATED TO 1.2V RAIL VIA 50 OHM.

* IN NORMAL MODE, OCM BOOTS FROM INTERNAL ROM.
* PCON COVERS CHAR CLOCK RANGES FROM 25MHZ TO 600MHZ.
* VDD12_ON IS ASSERTED UPON DETECTING AUX FROM A DP SOURCE OR HPD FROM AN HDMI SINK.

CONVERTER MODE:	600MW
SLEEP STATE:	15MW
CS POWER STATE: (TCLK_OFF)	5MW
CS POWER STATE: (VDD12_OFF)	0.1MW

UART (MAX) = 115.2KBPS
I2C (MAX) = 1MBPS (50KBPS)
SPI (MAX) = 75MHZ
INTERNAL OCM CK = 150MHZ
HDMI OUTPUT: 0.25 - 6.0 GBPS

HDMI_TX:
VSWING: 0 - 1200MV
PEMP: 0 - 5DB
DDC = 1 - 100KBPS

1V2	350MA TYPICAL
1V8	5MA TYPICAL
3V3	50MA TYPICAL

BOM_COST_GROUP=HDMI

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
197S00113	197S00109	YA800	CRYSTAL	

PAGE TITLE
DP TO HDMI PCON: MADEA

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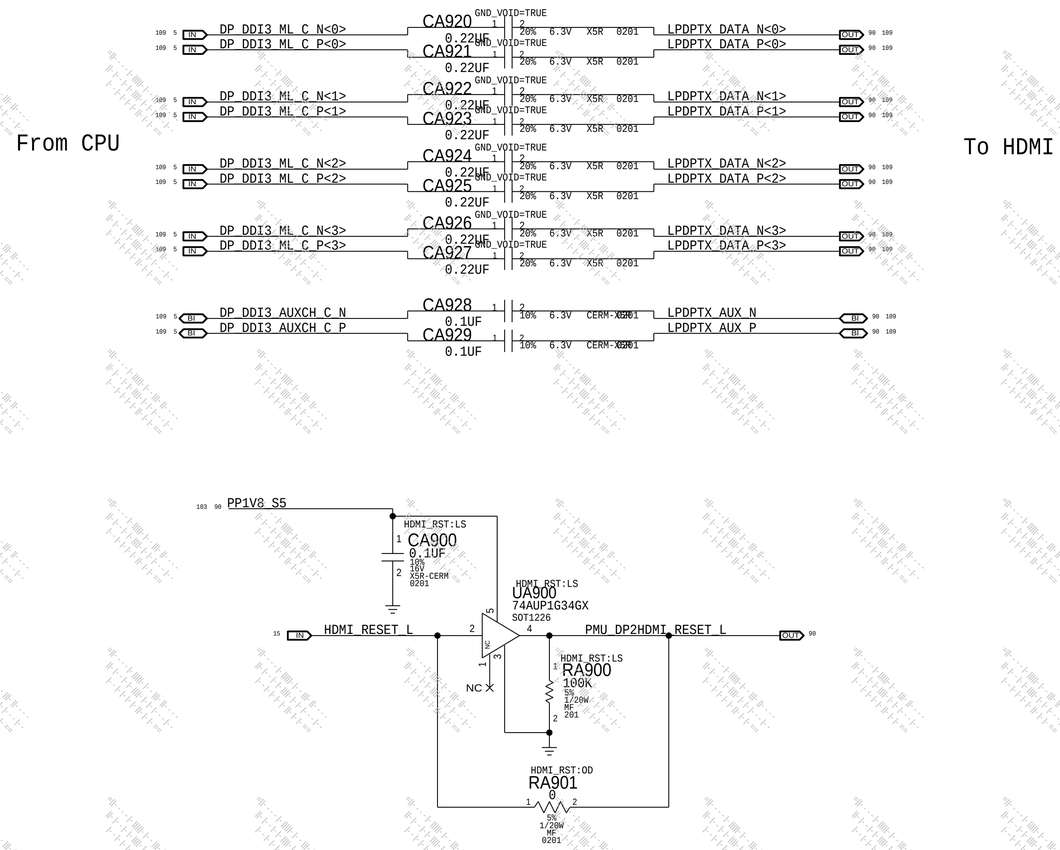
DDI interface AC Caps



BOM_COST_GROUP=HDMI

PAGE TITLE
HDMI PROJECT SUPPORT

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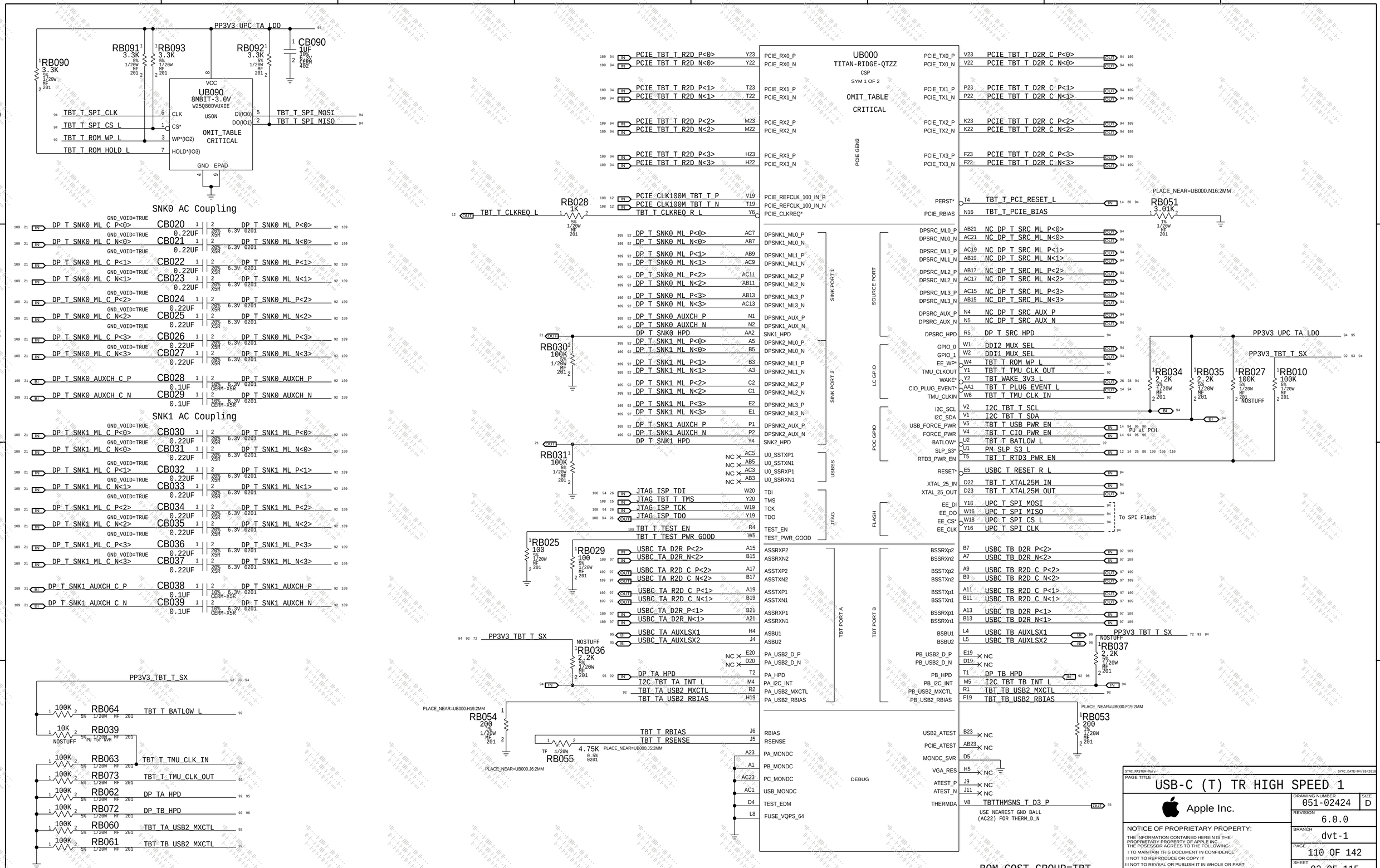
PP3V3_UPC_TA_LDO
RB090 3.3K
RB091 3.3K
RB093 3.3K
RB092 3.3K
CB090 1UF
UB090 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_ROM_WP_L
TBT_T_ROM_HOLD_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
UB000 TITAN-RIDGE-QTZZ CSP SYM 1 OF 2
OMIT_TABLE CRITICAL
PCIE GEN3
TBT_T_CLKREQ_L
RB028 1K
RB030 100K
RB031 100K
RB025 100
RB029 100
RB036 2.2K
RB054 200
RB055 4.75K
PP3V3_TBT_T_SX
RB064 100K
RB039 10K
RB063 100K
RB073 100K
RB062 100K
RB072 100K
RB060 100K
RB061 100K
SINK PORT 1
SINK PORT 2
USBSS
JTAG
TBT PORT A
SOURCE PORT
LC GPIO
POC GPIO
FLASH
TBT PORT B
DEBUG
PLACE_NEAR=UB000.N16:2MM
RB051 3.01K
PP3V3_UPC_TA_LDO
PP3V3_TBT_T_SX
RB034 2.2K
RB035 2.2K
RB027 100K
RB010 100K
NOSTUFF
PU at PCH
To SPI Flash
RB037 2.2K
RB053 200
BOM_COST_GROUP=TBT
USB-C (T) TR HIGH SPEED 1
Apple Inc.
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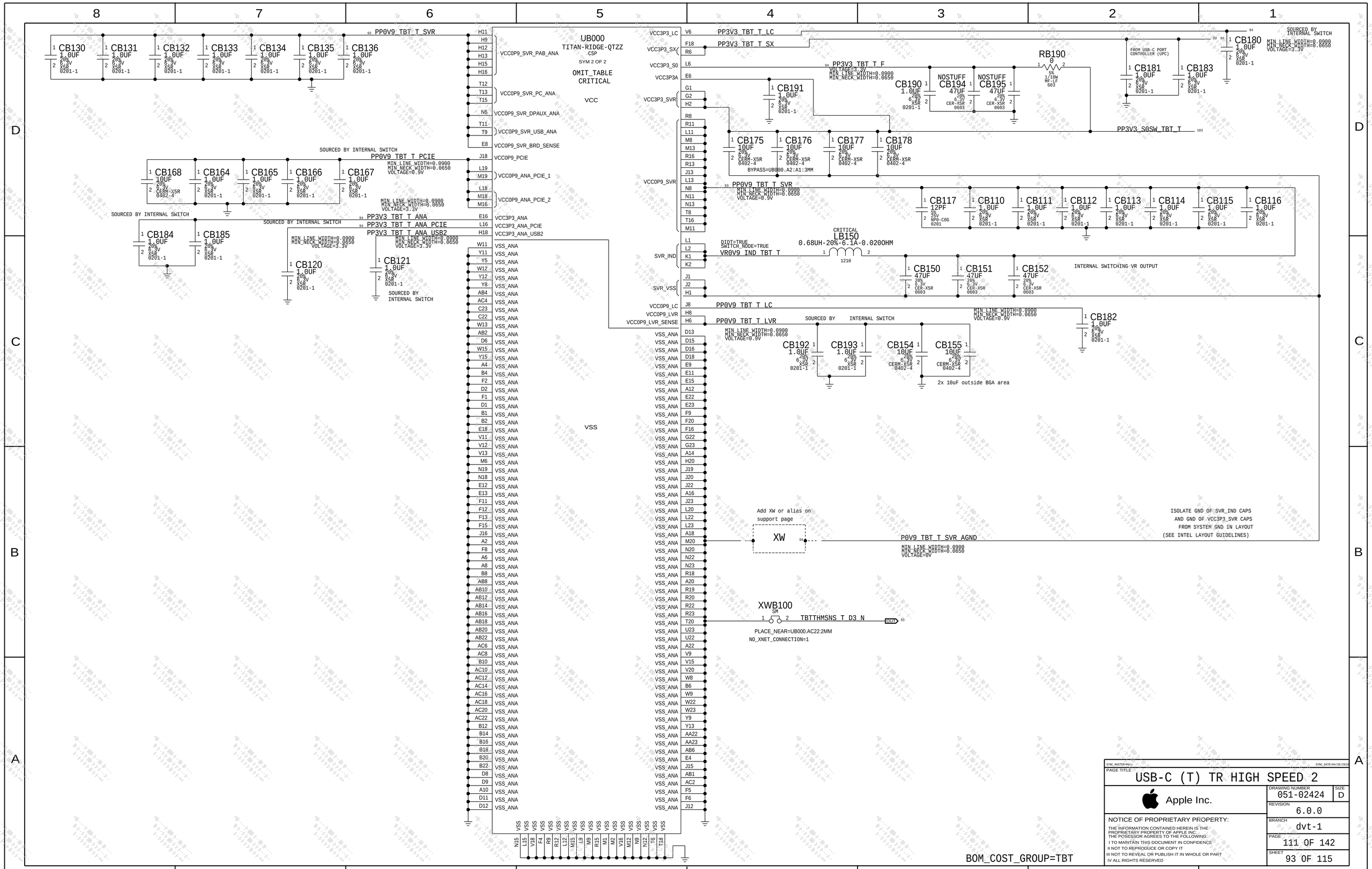
UB000
TITAN-RIDGE-QTZZ
CSP
SYM 2 OF 2
OMIT_TABLE
CRITICAL
VCC
VSS
PP0V9_TBT_T_SVR
CB130 1.0UF
CB131 1.0UF
CB132 1.0UF
CB133 1.0UF
CB134 1.0UF
CB135 1.0UF
CB136 1.0UF
VCC0P9_SVR_PAB_ANA
VCC0P9_SVR_PC_ANA
VCC0P9_SVR_DPAUX_ANA
VCC0P9_SVR_USB_ANA
VCC0P9_SVR_BRD_SENSE
VCC0P9_PCIE
VCC0P9_ANA_PCIE_1
VCC0P9_ANA_PCIE_2
VCC3P3_ANA
VCC3P3_ANA_PCIE
VCC3P3_ANA_USB2
VCC3P3_LC
VCC3P3_SX
VCC3P3_S0
VCC3P3A
VCC3P3_SVR
VCC0P9_SVR
SVR_IND
SVR_VSS
VCC0P9_LC
VCC0P9_LVR
VCC0P9_LVR_SENSE
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_T_PCIE
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=0.9V
VOLTAGE=3.3V
CB168 1.0UF
CB164 1.0UF
CB165 1.0UF
CB166 1.0UF
CB167 1.0UF
PP3V3_TBT_T_ANA
PP3V3_TBT_T_ANA_PCIE
PP3V3_TBT_T_ANA_USB2
CB184 1.0UF
CB185 1.0UF
CB120 1.0UF
CB121 1.0UF
PP3V3_TBT_T_LC
PP3V3_TBT_T_SX
PP3V3_TBT_T_F
VOLTAGE=3.3V
CB191 1.0UF
CB190 1.0UF
NOSTUFF CB194 47UF
NOSTUFF CB195 47UF
RB190 0
1/10W MF-1F 603
FROM USB-C PORT CONTROLLER (UPC)
CB181 1.0UF
CB183 1.0UF
CB180 1.0UF
SOURCED BY INTERNAL SWITCH
PP3V3_S0SW_TBT_T
CB175 10UF
CB176 10UF
CB177 10UF
CB178 10UF
BYPASS=UB000.AC22:2MM
PP0V9_TBT_T_SVR
CB117 12PF
CB110 1.0UF
CB111 1.0UF
CB112 1.0UF
CB113 1.0UF
CB114 1.0UF
CB115 1.0UF
CB116 1.0UF
DIDT=TRUE
SWITCH_NODE=TRUE
VR0V9_IND_TBT_T
CRITICAL
LB150
0.68UH-20%-6.1A-0.020OHM
1210
CB150 47UF
CB151 47UF
CB152 47UF
INTERNAL SWITCHING VR OUTPUT
PP0V9_TBT_T_LC
PP0V9_TBT_T_LVR
SOURCED BY INTERNAL SWITCH
CB192 1.0UF
CB193 1.0UF
CB154 10UF
CB155 10UF
2x 10uF outside BGA area
CB182 1.0UF
Add XW or alias on support page
XW
P0V9_TBT_T_SVR_AGND
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0650
VOLTAGE=0V
ISOLATE GND OF SVR_IND CAPS
AND GND OF VCC3P3_SVR CAPS
FROM SYSTEM GND IN LAYOUT
(SEE INTEL LAYOUT GUIDELINES)
XWB100
SM
TBTTHMSNS_T_D3_N
PLACE_NEAR=UB000.AC22:2MM
NO_XNET_CONNECTION=1
BOM_COST_GROUP=TBT
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-C (T) TR HIGH SPEED 2
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
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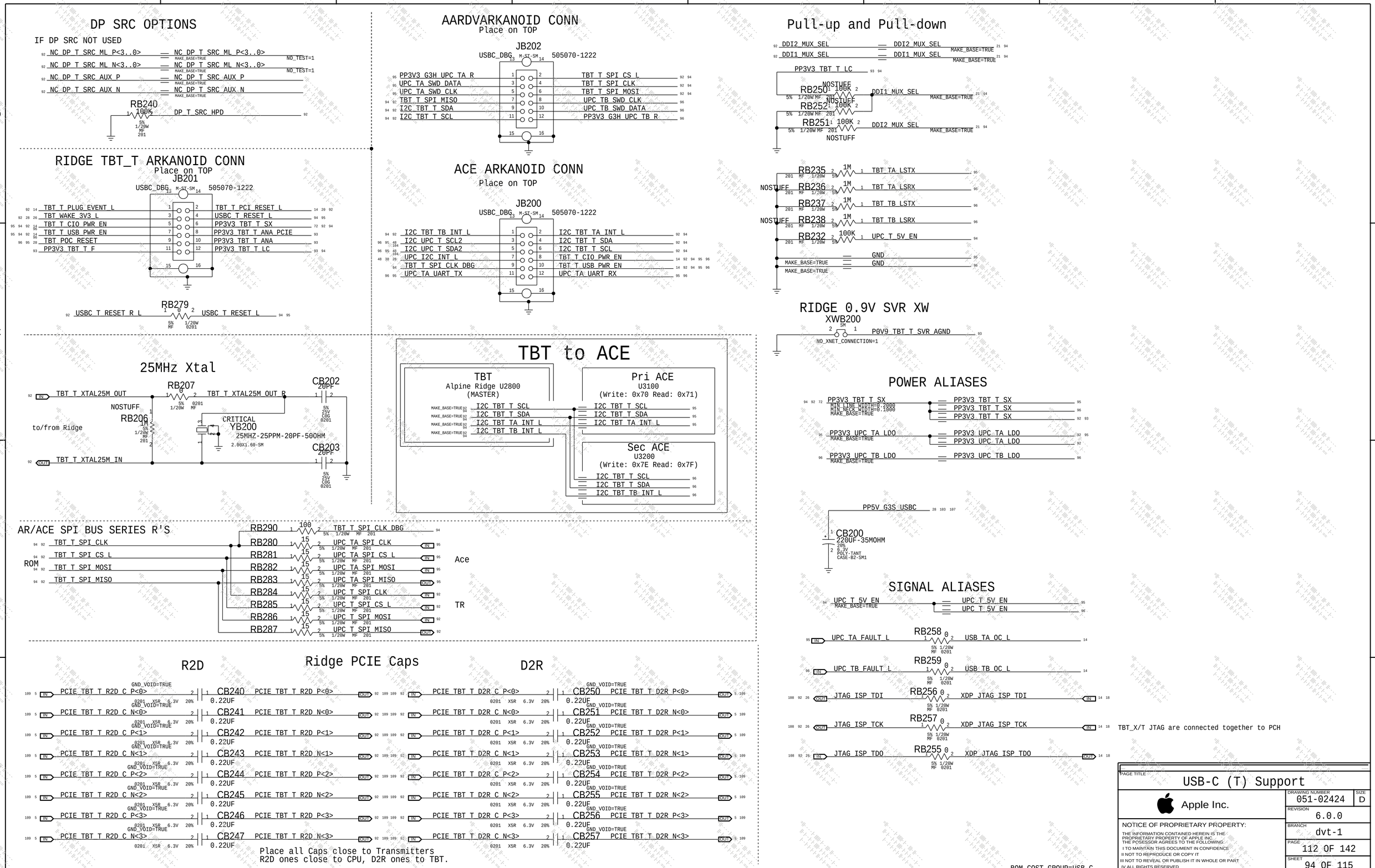
DP SRC OPTIONS
IF DP SRC NOT USED
NC_DP_T_SRC_ML_P<3..0>
NC_DP_T_SRC_ML_N<3..0>
NC_DP_T_SRC_AUX_P
NC_DP_T_SRC_AUX_N
MAKE_BASE=TRUE
NO_TEST=1
RB240
100K
DP_T_SRC_HPD
RIDGE TBT_T ARKANOID CONN
Place on TOP
JB201
USBC_DBG
M-ST-SM
505070-1222
TBT_T_PLUG_EVENT_L
TBT_WAKE_3V3_L
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
TBT_POC_RESET
PP3V3_TBT_T_F
TBT_T_PCI_RESET_L
USBC_T_RESET_L
PP3V3_TBT_T_SX
PP3V3_TBT_T_ANA_PCIE
PP3V3_TBT_T_ANA
PP3V3_TBT_T_LC
RB279
USBC_T_RESET_R_L
USBC_T_RESET_L
AARDVARKANOID CONN
Place on TOP
JB202
PP3V3_G3H_UPC_TA_R
UPC_TA_SWD_DATA
UPC_TA_SWD_CLK
TBT_T_SPI_MISO
I2C_TBT_T_SDA
I2C_TBT_T_SCL
TBT_T_SPI_CS_L
TBT_T_SPI_CLK
TBT_T_SPI_MOSI
UPC_TB_SWD_CLK
UPC_TB_SWD_DATA
PP3V3_G3H_UPC_TB_R
ACE ARKANOID CONN
Place on TOP
JB200
I2C_TBT_TB_INT_L
I2C_UPC_T_SCL2
I2C_UPC_T_SDA2
UPC_I2C_INT_L
TBT_T_SPI_CLK_DBG
UPC_TA_UART_TX
I2C_TBT_TA_INT_L
I2C_TBT_T_SDA
I2C_TBT_T_SCL
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
UPC_TA_UART_RX
Pull-up and Pull-down
DDI2_MUX_SEL
DDI1_MUX_SEL
PP3V3_TBT_T_LC
RB250
RB252
RB251
NOSTUFF
RB235
RB236
RB237
RB238
RB232
1M
100K
TBT_TA_LSTX
TBT_TA_LSRX
TBT_TB_LSTX
TBT_TB_LSRX
UPC_T_5V_EN
GND
RIDGE 0.9V SVR XW
XWB200
P0V9_TBT_T_SVR_AGND
NO_XNET_CONNECTION=1
25MHz Xtal
TBT_T_XTAL25M_OUT
TBT_T_XTAL25M_OUT_R
TBT_T_XTAL25M_IN
RB207
RB206
CB202
CB203
20PF
to/from Ridge
CRITICAL
YB200
25MHZ-25PPM-20PF-50OHM
2.00X1.60-SM
TBT to ACE
TBT
Alpine Ridge U2800
(MASTER)
Pri ACE
U3100
(Write: 0x70 Read: 0x71)
Sec ACE
U3200
(Write: 0x7E Read: 0x7F)
I2C_TBT_T_SCL
I2C_TBT_T_SDA
I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L
POWER ALIASES
PP3V3_TBT_T_SX
PP3V3_UPC_TA_LDO
PP3V3_UPC_TB_LDO
PP5V_G3S_USBC
CB200
220UF-35MOHM
POLY-TANT
CASE-B2-SM1
AR/ACE SPI BUS SERIES R'S
ROM
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
RB290
RB280
RB281
RB282
RB283
RB284
RB285
RB286
RB287
100
15
TBT_T_SPI_CLK_DBG
UPC_TA_SPI_CLK
UPC_TA_SPI_CS_L
UPC_TA_SPI_MOSI
UPC_TA_SPI_MISO
UPC_T_SPI_CLK
UPC_T_SPI_CS_L
UPC_T_SPI_MOSI
UPC_T_SPI_MISO
Ace
TR
SIGNAL ALIASES
UPC_T_5V_EN
UPC_TA_FAULT_L
UPC_TB_FAULT_L
JTAG_ISP_TDI
JTAG_ISP_TCK
JTAG_ISP_TDO
RB258
RB259
RB256
RB257
RB255
USB_TA_OC_L
USB_TB_OC_L
XDP_JTAG_ISP_TDI
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDO
TBT_X/T JTAG are connected together to PCH
Ridge PCIE Caps
R2D
D2R
PCIE_TBT_T_R2D_C_P<0>
PCIE_TBT_T_R2D_C_N<0>
PCIE_TBT_T_R2D_C_P<1>
PCIE_TBT_T_R2D_C_N<1>
PCIE_TBT_T_R2D_C_P<2>
PCIE_TBT_T_R2D_C_N<2>
PCIE_TBT_T_R2D_C_P<3>
PCIE_TBT_T_R2D_C_N<3>
PCIE_TBT_T_R2D_P<0>
PCIE_TBT_T_R2D_N<0>
PCIE_TBT_T_R2D_P<1>
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PCIE_TBT_T_R2D_N<3>
PCIE_TBT_T_D2R_C_P<0>
PCIE_TBT_T_D2R_C_N<0>
PCIE_TBT_T_D2R_C_P<1>
PCIE_TBT_T_D2R_C_N<1>
PCIE_TBT_T_D2R_C_P<2>
PCIE_TBT_T_D2R_C_N<2>
PCIE_TBT_T_D2R_C_P<3>
PCIE_TBT_T_D2R_C_N<3>
PCIE_TBT_T_D2R_P<0>
PCIE_TBT_T_D2R_N<0>
PCIE_TBT_T_D2R_P<1>
PCIE_TBT_T_D2R_N<1>
PCIE_TBT_T_D2R_P<2>
PCIE_TBT_T_D2R_N<2>
PCIE_TBT_T_D2R_P<3>
PCIE_TBT_T_D2R_N<3>
CB240
CB241
CB242
CB243
CB244
CB245
CB246
CB247
CB250
CB251
CB252
CB253
CB254
CB255
CB256
CB257
0.22UF
GND_VOID=TRUE
Place all Caps close to Transmitters
R2D ones close to CPU, D2R ones to TBT.
BOM_COST_GROUP=USB-C
PAGE TITLE
USB-C (T) Support
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
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T PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY

PPVBUS_USBC_TA
PP1V8_SLPS2R — 1V8 SOURCE FOR ACE 1V8 GPIO
PP3V3_G3H — RB389 0 5% 1/16W MF-LF 402 — PP3V3_G3H_UPC_TA_R — 12V IS TO FLASH THE ACE ONLY — VOLTAGE=3.3V
PP12V_MAIN — RB399 0 5% 1/16W MF-LF 402 — PPHV_USBC_TA — VOLTAGE=12V
ACE LDO CAN DRAW UP TO 5.9 MA WHILE PROGRAMMING OTP
PP5V_G3S_USBC

CB398 1.0UF 10% 25V X6S 0402
CB399 1UF 10% 35V X5R 0402
CB300 10UF 20% 6.3V CERM-X5R 0402-1
CB307 1.0UF 20% 6.3V X5R 0201-1
CB301 1UF 10% 35V X5R 0402
DB300 X3-WLB1608-1 SDM2U40CSP

PP3V3_UPC_TA_LDO — VOLTAGE=3.3V — VOUT_3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP3V3_TBT_T_SX
PP1V8_UPC_TA_LDOA — VOLTAGE=1.8V
PP1V8_UPC_TA_LDOD — VOLTAGE=1.8V
PP1V1_UPC_TA_LDO_BMC — VOLTAGE=1.1V

CB308 10UF 20% 6.3V CERM-X5R 0402-1
CB304 2.2UF 20% 4V X5R-CERM 0201
CB305 1.0UF 20% 6.3V X5R 0201-1
CB306 0.47UF 10% 6.3V CERM-X5R 0201

PP_5V0_A11, PP_5V0_B11, PP_5V0_C11, PP_5V0_D11, PP_HV_A6, PP_HV_A7, PP_HV_A8, PP_HV_B7, PP_CABLE_H10, VBUS_H11, VBUS_H10, VBUS_H11, VBUS_K11, VIN_3V3_H1, VDDIO_B1, LDO_3V3_G1, VOUT_3V3_H2, LDO_1V8A_K1, LDO_1V8D_A2, LDO_BMC_E1

CRITICAL
OMIT_TABLE
UB300
CD3215C00
PBGA
TPS65983
C0 SILICON

MREST HIGH FORCES F11 RESET LOW
ACTIVE LOW RESET OUTPUT
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 EVEN IN PRODUCTION
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS
USE GPIO5 FOR PMU RESET AFTER BOOT.
BUSPOWERZ CONTROLS BUS POWER PATH FOR PP_EXT_IT MUST BE < 0.8 V
I2C_ADDR CONTROLS ADDR BITS 3,2,1 J135: GND I2C_ADDR ON PRIMARY ONLY
R_OSC NEEDS NEEDS 0.1% RES
CKPLUS_WAIVE=TERMSHORTED
I2C BUS 1 IS TBT / ACES
I2C BUS 2 IS SMC / ACES
Portable: rear connector->TBT ROM, front connector->GND
Desktop: XA_SPI -> TBT ROM, XB_SPI -> GND

Pin	Net	Dir	Voltage
F11	MRESET	(DIO)	(3V3)
F13	RESET*	(DIO)	(3V3)
B2	GPIO0	(DIO)	
C2	GPIO1	(DIO)	(1V8)
D10	GPIO2	(DIO)	(3V3)
G11	GPIO3	(DIO)	(3V3)
C10	GPIO4	(DIO)	(3V3)
E10	GPIO5	(DIO)	(1V8)
G10	GPIO6	(DIO)	(3V3)
D7	GPIO7	(DIO)	(1V8)
H6	GPIO8	(DIO)	(3V3)
F10	BUSPOWERZ	(AI)	
F1	I2C_ADDR	(AIO)	
G2	R_OSC	(AIO)	
E4	DEBUG_CTL1	(DIO)	(DM2)
D5	DEBUG_CTL2	(DIO)	
D1	I2C_SDA1	(DIO)	
D2	I2C_SCL1	(DIO)	(3V3)
C3	I2C_IRQ1*	(HIZ)	
A5	I2C_SDA2	(DIO)	
B5	I2C_SCL2	(DIO)	(1V8)
B6	I2C_IRQ2*	(HIZ)	
A3	SPI_CLK	(DO)	
B4	SPI_MOSI	(DO)	
A4	SPI_MISO	(DI)	
B3	SPI_SSZ	(DO)	
F4	SWD_DATA	(DIO)	
G4	SWD_CLK	(DI)	
F2	UART_RX	(DI)	
E2	UART_TX	(DO)	
L4	LSX_R2P	(DI)	(NOT USED)
K4	LSX_P2R	(DO)	
L5	USB_RP_P	(AIO)	
K5	USB_RP_N	(AIO)	
J1	AUX_P	(AIO)	
J2	AUX_N	(AIO)	
L2	DEBUG1	(AIO)	(1V8)
K2	DEBUG2	(AIO)	
L3	DEBUG3	(AIO)	
K3	DEBUG4	(AIO)	

DIGITAL CORE IO AND CONTROL — HV FET/SENSE — TYPE-C — PORT MUX

Pin	Net	Dir
H7	SS	(AO)
B10	SENSEP	(AI)
A10	SENSEN	(AI)
B9	HV_GATE1	(AO)
A9	HV_GATE2	(AO)
L9	C_CC1	(AIO)
L10	C_CC2	(AIO)
K9	RPD_G1	(AIO)
K10	RPD_G2	(AIO)
K6	C_USB_TP	(AIO)
L6	C_USB_TN	(AIO)
K7	C_USB_BP	(AIO)
L7	C_USB_BN	(AIO)
K8	C_SBU1	(AIO)
L8	C_SBU2	(AIO)
L11	NC	

UPC_TA_SS — CB309 0.47UF 10% 6.3V CERM-X5R 0201
NC_UPC_TA_HV_GATE1
NC_UPC_TA_HV_GATE2
USBC_TA_CC1 — CB314 220PF 10% 16V CER-X7R 0201
USBC_TA_CC2 — CB313 220PF 10% 16V CER-X7R 0201
USBC_TA_USB_TOP_P
USBC_TA_USB_TOP_N
USBC_TA_USB_BOT_P
USBC_TA_USB_BOT_N
USBC_TA_SBU1
USBC_TA_SBU2

SOFT START RAMP RATE = 9 * ISS / CSS
ISS = 7 UA NOMIAL, 5.5 MA MIN, 8.5 MA MAX
SHORT SENSE INPUTS TO VBUS WHEN UNUSED
FLOAT HV GATE OUTPUTS WHEN UNUSED
C_CC1 AND C_CC2 PINS USED TO DELIVER POWER TO ACTIVE CIRCUITRY INSIDE A CONNECTED CABLE AND OUTPUT USB-PD DATA TO THE CABLE AND CONNECTED DEVICE
J137 HAS NO BATTERY, SO RPD CONNECT TO GND
PORT SIDE USB TOP PAIR
PORT SIDE USB BOTTOM PAIR
PORT SIDE USB SIDEBAND
PIN L11 NC OR GND TO DISSIPATE HEAT

RB302 0 5% 1/20W MF 0201
RB303 15K 0.1% 1/20W TF-LF 0201

PCH USB2
USB_UPC_TA_P — PLACE_NEAR=UB300.L5:5mm
USB_UPC_TA_N — PLACE_NEAR=UB300.K5:5mm
LB300 90-OHM-0.1A EXCACE-SYM_V01-1
TPB300 TP-P5 A
TPB301 TP-P5 A
USB_UPC_TA_FP
USB_UPC_TA_FN
USBC_TA_AUXLSX1
USBC_TA_AUXLSX2
SMC_DEBUGPRT_TX
SMC_DEBUGPRT_RX
UPC_TA_DBG3
UPC_TA_DBG4
RB356 100K 5% 1/20W MF 201
RB357 100K 5% 1/20W MF 201

GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

PULL RB309 AND RB308 UP TO ACES LDOS FOR 1ST RIDGE'S ACES
PULL THEM DOWN TO GND FOR 2ND RIDGE'S ACES
RB309 1M 5% 1/20W MF 201 — I2C_UPC_TA_DBG_CTL_SCL — CKPLUS_WAIVE=I2C_PULLUP
RB308 1M 5% 1/20W MF 201 — I2C_UPC_TA_DBG_CTL_SDA — CKPLUS_WAIVE=I2C_PULLUP
RB305 1M 5% 1/20W MF 201 — UPC_TA_UART_RX
RB310 1M 5% 1/20W MF 201 — UPC_TA_GPIO1 — NOSTUFF

NOTE:
DEBUG MUX IS CONNECTED TO PRIMARY ACE OF 1ST RIDGE (XA ACE)
R3752-R3755, R3790-R3792 ARE OPTIONAL

BOM_COST_GROUP=USB-C

04/26/2018 Mary
NOT SYNCED TO OTHER PLATFORMS
PAGE_TITLE=USB-C (T) PORT CONTROLLER A

Apple Inc.

PAGE TITLE	USB-C (T) PORT CONTROLLER A
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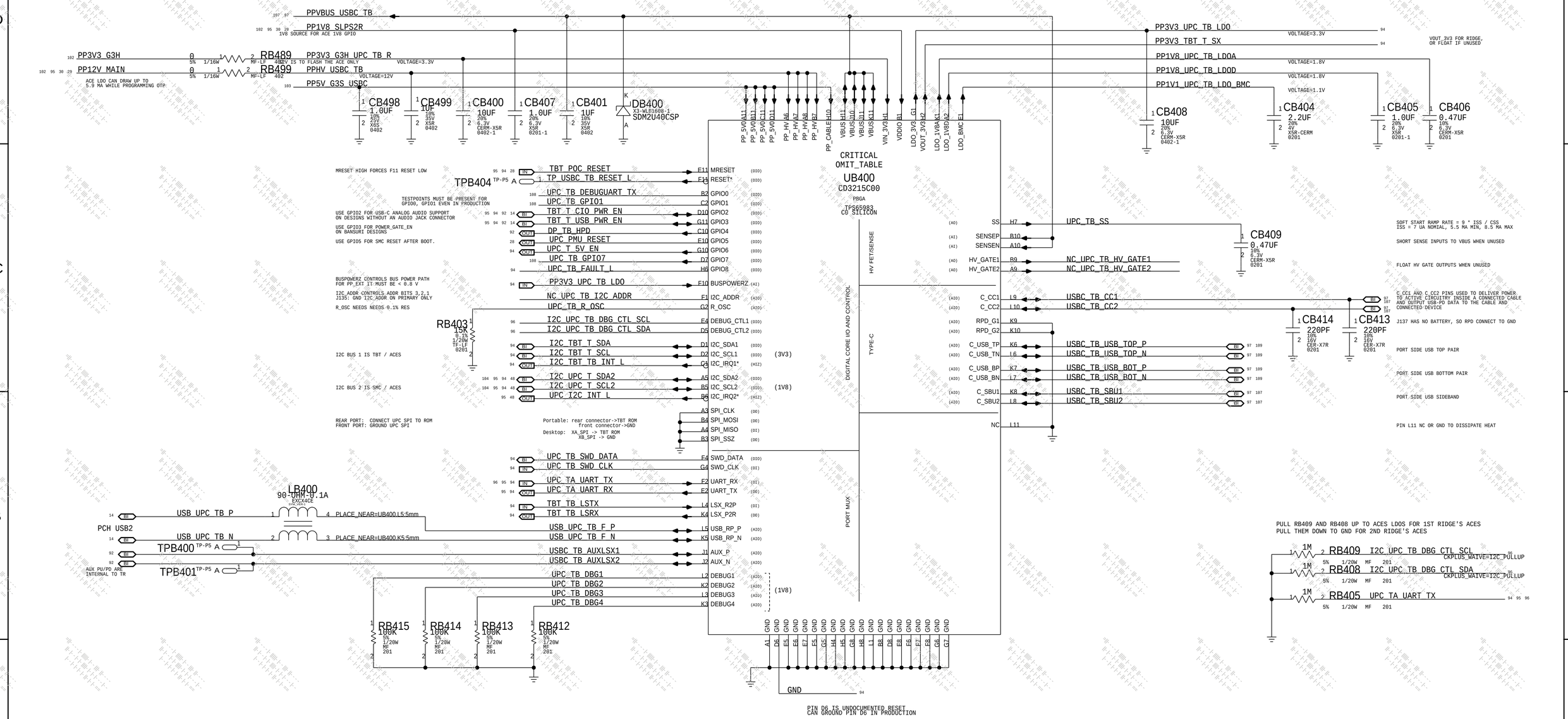
T SECONDARY ACE USB-C PORT CONTROLLER (UPC)



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Mary
SYNC_DATE=04/26/2018

PAGE TITLE: PAGE_TITLE=USB-C (T) PORT CONTROLLER B

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DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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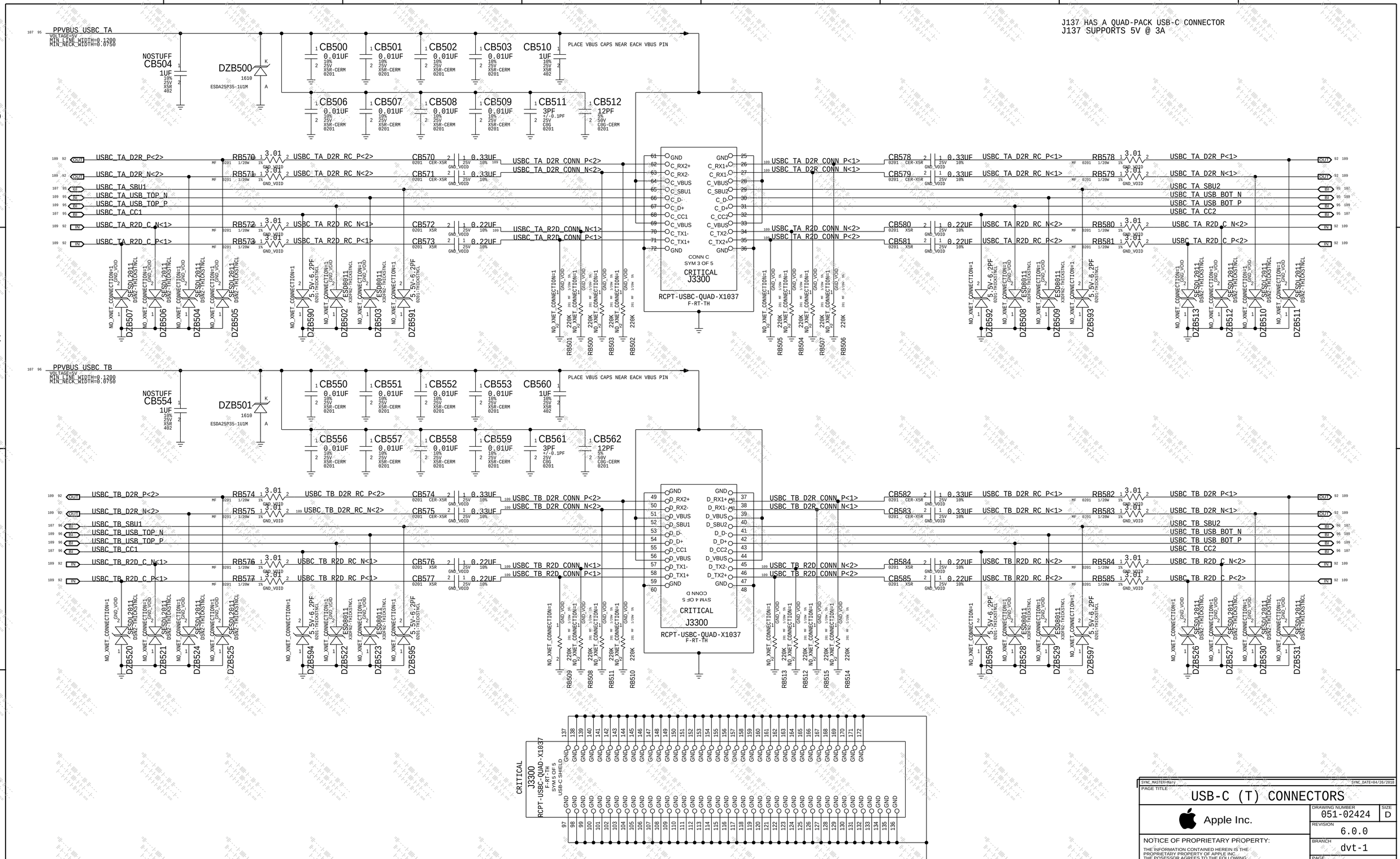

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: USB-C (T) CONNECTORS

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DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

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Place Holder

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mac SYNC_DATE=06/07/2016

PAGE TITLE
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BOM_COST_GROUP=DEBUG

PAGE TITLE	Empty
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
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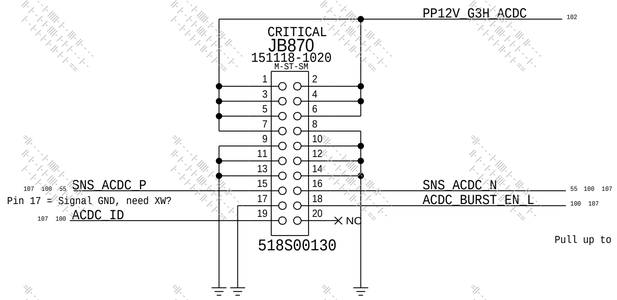
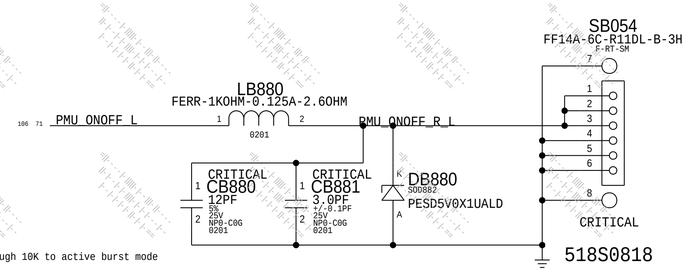
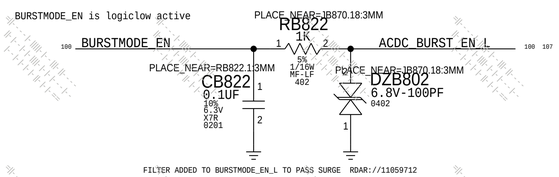
MLB Power button connector

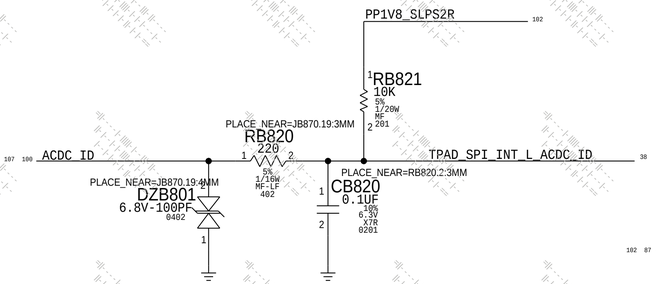


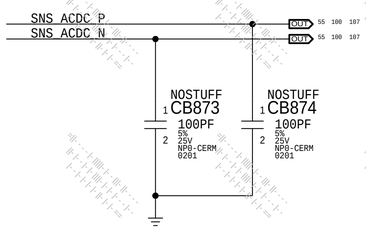
ACDC_ID: From PSU to inform vendor A or B.
10K PD to pin 17 or Open.

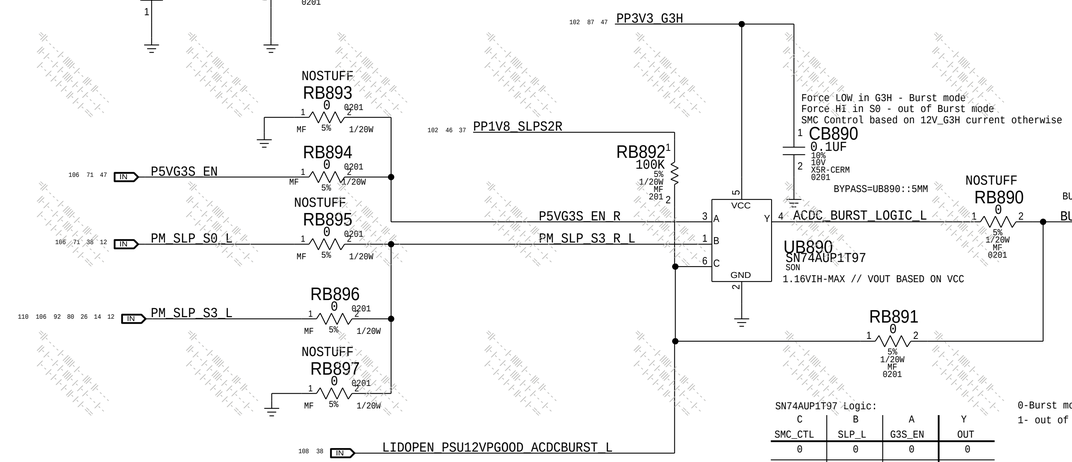


Pull up to 3.3V through 10K to active burst mode







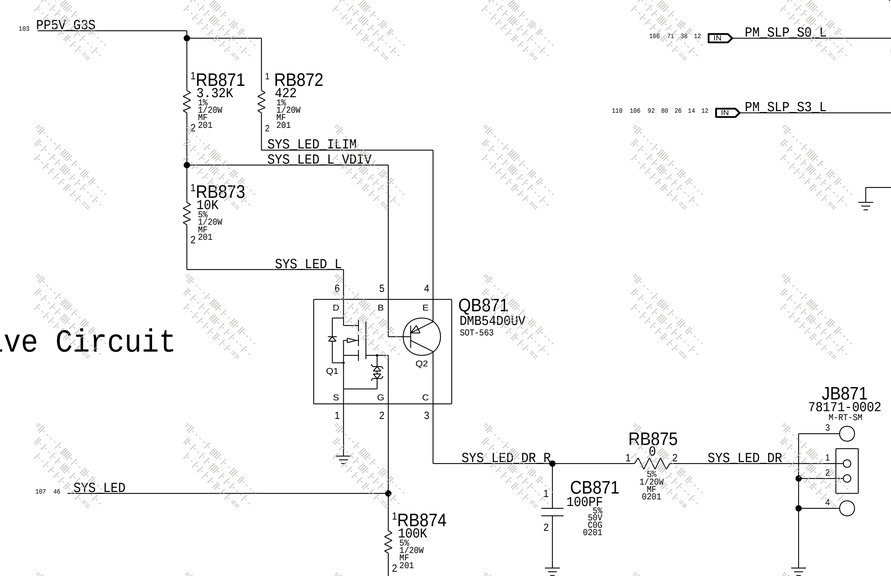


SN74AUP1T97 Logic:

C	B	A	Y	
SMC_CTL	SLP_L	G3S_EN	OUT	
0	0	0	0	
1	0	0	0	
0	1	0	1	Invalid system state
1	1	0	0	(Don't Care)
0	0	1	0	
1	0	1	1	
0	1	1	1	
1	1	1	1	

0-Burst mode
1- out of Burst mode

SIL LED Drive Circuit



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER:Mary SYNC_DATE:04/26/2018

PAGE TITLE: POWER INPUT FROM AC/DC 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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12V PBUS Rails

100 PP12V_G3H_ACDC
- PP12V_G3H_ACDC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=12V, MAKE_BASE=TRUE — 106
- PP12V_G3H_ACDC — 51
- PP12V_G3H_ACDC — 104

51 PP12V_MAIN
- PP12V_MAIN — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=12V, MAKE_BASE=TRUE — 105 106
- PP12V_MAIN — 63
- PP12V_MAIN — 56
- PP12V_MAIN — 53
- PP12V_MAIN — 71
- PP12V_MAIN — 29 30 95 96
- PP12V_MAIN — 51
- PP12V_MAIN — 51
- PP12V_MAIN — 57
- PP12V_MAIN — 47
- PP12V_MAIN — 104
- PP12V_MAIN — 60

CPU High Side Rails

51 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.7000, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPBUS_HS_CPU — 63 64 65 66 73
- PPBUS_HS_CPU — 67
- PPBUS_HS_CPU — 104 105

3V3_G3H High Side Rails

51 PP12V_G3H_VIN_P3V3_G3H
- PP12V_G3H_VIN_P3V3_G3H — MIN_LINE_WIDTH=0.1930, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PP12V_G3H_VIN_P3V3_G3H — 68
- PP12V_G3H_VIN_P3V3_G3H — 104 105

5V_G3S High Side Rails

51 PP12V_G3H_VIN_P5V_G3S
- PP12V_G3H_VIN_P5V_G3S — MIN_LINE_WIDTH=0.1930, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PP12V_G3H_VIN_P5V_G3S — 68
- PP12V_G3H_VIN_P5V_G3S — 104 105

12V to NAND 2V7 VR Rails

53 PPVIN_G3H_P2V7
- PPVIN_G3H_P2V7 — MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.0720, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPVIN_G3H_P2V7 — 79

12V to ENET VR Rails

56 PPVIN_ENET_P0V85
- PPVIN_ENET_P0V85 — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPVIN_ENET_P0V85 — 87
- PPVIN_ENET_P0V85 — 104

3V3 G3H Rails

68 PP3V3_G3H
- PP3V3_G3H — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 105 106
- PP3V3_G3H — 54
- PP3V3_G3H — 102
- PP3V3_G3H — 54
- PP3V3_G3H — 56
- PP3V3_G3H — 72
- PP3V3_G3H — 72
- PP3V3_G3H — 102
- PP3V3_G3H — 29
- PP3V3_G3H — 30
- PP3V3_G3H — 95
- PP3V3_G3H — 96
- PP3V3_G3H — 47 87 100
- PP3V3_G3H — 53
- PP3V3_G3H — 110
- PP3V3_G3H — 28
- PP3V3_G3H — 67
- PP3V3_G3H — 19
- PP3V3_G3H — 73
- PP3V3_G3H — 70
- PP3V3_G3H — 113
- PP3V3_G3H — 70
- PP3V3_G3H — 113
- PP3V3_G3H — 48
- PP3V3_G3H — 72

3V3_G3H SSD Rail

53 PP3V3_G3H_SSD
- PP3V3_G3H_SSD — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 106
- PP3V3_G3H_SSD — 79 105
- PP3V3_G3H_SSD — 104

CPU Rails

64 PPVCC_S0_CPU_REG
- PPVCC_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCC_S0_CPU_REG — 6 8 56
- PPVCC_S0_CPU_REG — 10
- PPVCC_S0_CPU_REG — 104 105

66 PPVCCSA_S0_CPU_REG
- PPVCCSA_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCCSA_S0_CPU_REG — 8 56
- PPVCCSA_S0_CPU_REG — 11

65 PPVCCGT_S0_CPU_REG
- PPVCCGT_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCCGT_S0_CPU_REG — 8 56
- PPVCCGT_S0_CPU_REG — 10
- PPVCCGT_S0_CPU_REG — 104

CPU VCCIO Rails

54 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=0.95V — 106
- PPVCCIO_S0_CPU — 5 8
- PPVCCIO_S0_CPU — 11
- PPVCCIO_S0_CPU — 104 105

BUCK0 VDD SoC CPU

69 PPVDDCPU_AWAKE_SOC
- PPVDDCPU_AWAKE_SOC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.06V — 106
- PPVDDCPU_AWAKE_SOC — 41 105 112

BUCK1 VDD SoC CPU SRAM

69 PPVDDCPUSRAM_AWAKE
- PPVDDCPUSRAM_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.06V — 106
- PPVDDCPUSRAM_AWAKE — 41

BUCK2 SoC VDD_SOC

69 PP0V82_SLPDDR
- PP0V82_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BE=TRUE, VOLTAGE=.82V — 106
- PP0V82_SLPDDR — 41 105 112

V3P3_SW1 USB

70 PP3V3_AWAKE
- PP3V3_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=3.3V — 106
- PP3V3_AWAKE — 43

PMIC LDO2 PCIE_REFBUF/PLL

70 PP1V2_AWAKE
- PP1V2_AWAKE — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.2V — 106
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43

PMIC LDO0 - VDD_LOW

70 PP0V8_SLPS2R
- PP0V8_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=0.8V, MAKE_BASE=TRUE — 106
- PP0V8_SLPS2R — 42

RTC Rails (PMIC LDO 1)

19 PP3V0_G3H_RTC
- PP3V0_G3H_RTC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3V, MAKE_BASE=TRUE — 106
- PP3V0_G3H_RTC — 12 16 17

Calpe 3V3 VDD Rail

54 PP3V3_G3H_PMU
- PP3V3_G3H_PMU — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 107
- PP3V3_G3H_PMU — 69
- PP3V3_G3H_PMU — 70
- PP3V3_G3H_PMU — 70
- PP3V3_G3H_PMU — 71
- PP3V3_G3H_PMU — 70

3V3_G3H ENET Rail

56 PP3V3_G3H_ENET
- PP3V3_G3H_ENET — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 85 106
- PP3V3_G3H_ENET — 72 86 87

3V3 ENET Rail(Pass FET)

105 84 83 82 81 80 72 19 PP3V3_ENET
- PP3V3_ENET — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 106
- PP3V3_ENET — 104

BUCK3 AOP/SMC/VDD1(1V8)

69 PP1V8_SLPS2R
- PP1V8_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE — 84 106
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 113
- PP1V8_SLPS2R — 69 (Buck3_SW input, 1V8 G3S input)
- PP1V8_SLPS2R — 70
- PP1V8_SLPS2R — 71
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 45
- PP1V8_SLPS2R — 45
- PP1V8_SLPS2R — 37 46 100
- PP1V8_SLPS2R — 29 30 95 96 (1V8_SLPS2R MISC)
- PP1V8_SLPS2R — 110
- PP1V8_SLPS2R — 100

BUCK3_SW1(1V8)

69 PP1V8_AWAKE
- PP1V8_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE — 106
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 71
- PP1V8_AWAKE — 45
- PP1V8_AWAKE — 28 40 45 46
- PP1V8_AWAKE — 45 (1V8_AWAKE MISC)
- PP1V8_AWAKE — 113
- PP1V8_AWAKE — 104

BUCK4 SDRAM VDD2 (1V1)

69 PP1V1_SLPS2R
- PP1V1_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE — 106
- PP1V1_SLPS2R — 42
- PP1V1_SLPS2R — 43
- PP1V1_SLPS2R — 70 (0V8 LDO0 input)
- PP1V1_SLPS2R — 69 (Buck4_SW input)
- PP1V1_SLPS2R — 70 (1V1 SLPDDR SW input)

1V1 SLPDDR SOC VDDIO DDR (SoC Transition State)

70 PP1V1_SLPDDR
Source from 1V1_SLPS2R
EN by PMIC.GPIO
- PP1V1_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE — 106
- PP1V1_SLPDDR — 42 105
- PP1V1_SLPDDR — 37
- PP1V1_SLPDDR — 42
- PP1V1_SLPDDR — 43

BUCK5 VDD_FIXED

69 PP0V9_SLPDDR
- PP0V9_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=0.9V, MAKE_BASE=TRUE — 106
- PP0V9_SLPDDR — 42 105
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42

LDO1 for RTC

70 19 PPVRTC_G3_PCH_REG_R
- PPVRTC_G3_PCH_REG_R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.0V, MAKE_BASE=TRUE

1.1V PRIM FOR XTAL

17 16 PP1V_PRIM_PCH_VCCAXTAL_F
- PP1V_PRIM_PCH_VCCAXTAL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE

1.1V PRIM FOR PLL

17 16 PP1V_PRIM_PCH_VCCAPLL_F
- PP1V_PRIM_PCH_VCCAPLL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE

1.1V PRIM FOR MPHY_PLL

17 16 PP1V_PRIM_PCH_VCCAMPHYPLL_F
- PP1V_PRIM_PCH_VCCAMPHYPLL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1V, MAKE_BASE=TRUE

BOM_COST_GROUP=PLATFORM POWER

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Apple Inc.	DRAWING NUMBER 051-02424 / SIZE D
	REVISION 6.0.0
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1V S5 Rails

69 PP1V_PRIM
PP1V_PRIM
MIN_LINE_WIDTH=0.0700
MIN_NECK_WIDTH=0.0650
VOLTAGE=1.0V
MAKE_BASE=TRUE
106
PP1V_PRIM 69
PP1V_PRIM 16 17
PP1V_PRIM 16
PP1V_PRIM 16
PP1V_PRIM 16
PP1V_PRIM 16 17
PP1V_PRIM 17
These 3x rails need filter
PP1V_PRIM
PP1V_PRIM 17
PP1V_PRIM 17
PP1V_PRIM 18
PP1V_PRIM 112
PP1V_PRIM 47
PP1V_PRIM 16
PP1V_PRIM 104

1V S3 Rails

69 PP1V_S3
PP1V_S3
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.0V
MAKE_BASE=TRUE
106
PP1V_S3 8 11 45
PP1V_S3 8 11
PP1V_S3 71
PP1V_S3 63
PP1V_S3 6 13 20
PP1V_S3 45

1V2 S5 Rails

69 PP1V2_PRIM
PP1V2_PRIM
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_PRIM 90

1V2 S3 Rails

67 PP1V2_S3
PP1V2_S3
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE
106 107
PP1V2_S3 23
PP1V2_S3 24
PP1V2_S3 22
PP1V2_S3 67
PP1V2_S3 12
PP1V2_S3 105
PP1V2_S3 8
PP1V2_S3 11
PP1V2_S3 72

72 PP1V2_S0SW
PP1V2_S0SW
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE
106
PP1V2_S0SW 8 11

0V6 Rails

23 22 PP0V6_S3_MEM_VREFCAA
PP0V6_S3_MEM_VREFCAA
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0.6V
MAKE_BASE=TRUE

24 22 PP0V6_S3_MEM_VREFCAB
PP0V6_S3_MEM_VREFCAB
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0.6V
MAKE_BASE=TRUE

2V5 VPP Rails

67 PP2V5_S3
PP2V5_S3
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=2.5V
MAKE_BASE=TRUE
107
PP2V5_S3 52

52 PP2V5_S3_VPP
PP2V5_S3_VPP
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=2.5V
MAKE_BASE=TRUE
107
PP2V5_S3_VPP 23
PP2V5_S3_VPP 24
PP2V5_S3_VPP 23 50
PP2V5_S3_VPP 24
PP2V5_S3_VPP 47

VTT Rails

67 PPDDRVTT_S0_MEM
PPDDRVTT_S0_MEM
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.2V
MAKE_BASE=TRUE
106 107
PPDDRVTT_S0_MEM 23
PPDDRVTT_S0_MEM 24

Digital Ground

GND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0V

1V8 G3S Rails

69 PP1V8_G3S
PP1V8_G3S
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V
MAKE_BASE=TRUE
59 106
PP1V8_G3S 34 35 107
PP1V8_G3S 47 57
PP1V8_G3S 68
PP1V8_G3S 60
PP1V8_G3S 49

1V8 S5 Rails

69 PP1V8_S5
PP1V8_S5
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.8V
MAKE_BASE=TRUE
106
PP1V8_S5 47
PP1V8_S5 12 13 15 16 17 50
PP1V8_S5 12 16 17 38
PP1V8_S5 16
PP1V8_S5 13 16 17
PP1V8_S5 18
PP1V8_S5 35 50 71
PP1V8_S5 45
PP1V8_S5 16 17
PP1V8_S5 15 72
PP1V8_S5 90 91
PP1V8_S5 55
PP1V8_S5 55
PP1V8_S5 47 63 67 73
PP1V8_S5 20
PP1V8_S5 113
PP1V8_S5 45
PP1V8_S5 45

5V G3S Rails

68 PP5V_G3S
PP5V_G3S
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=5V
MAKE_BASE=TRUE
87 106
PP5V_G3S 56
PP5V_G3S 56
PP5V_G3S 88
Modified for HDMI
PP5V_G3S 63
PP5V_G3S 64 65 66 73
PP5V_G3S 67
PP5V_G3S 113
PP5V_G3S 104 105
PP5V_G3S 100

USBC 5V Rails

56 PP5V_G3S_USBC
PP5V_G3S_USBC
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=5V
MAKE_BASE=TRUE
28 94 107
PP5V_G3S_USBC 29
PP5V_G3S_USBC 30
PP5V_G3S_USBC 95
PP5V_G3S_USBC 96
PP5V_G3S_USBC 104

USBA 5V Rails

56 PP5V_G3S_USBA
PP5V_G3S_USBA
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=5V
MAKE_BASE=TRUE
107
PP5V_G3S_USBA 62

3V3 G3S Rails

72 PP3V3_G3S
PP3V3_G3S
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
MAKE_BASE=TRUE
59 86 106
PP3V3_G3S 56
PP3V3_G3S 54
PP3V3_G3S 51
PP3V3_G3S 52
PP3V3_G3S 52 53 54 56
PP3V3_G3S 51 56
Sensor Rails

3V3 G3S Harpoon Rails

56 PP3V3_G3S_WLANBT
PP3V3_G3S_WLANBT
MIN_LINE_WIDTH=0.1010
MIN_NECK_WIDTH=0.0650
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_G3S_WLANBT 35 107
PP3V3_G3S_WLANBT 34

3V3 S5 Rails

70 PP3V3_S5
PP3V3_S5
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
MAKE_BASE=TRUE
82 106
PP3V3_S5 16 17 20
PP3V3_S5 12 16 17 71
PP3V3_S5 15 16 17
PP3V3_S5 14 16 17
PP3V3_S5 13 15 16 17
PP3V3_S5 12 15 16 17
GPPD is 1V8?
PP3V3_S5 72
PP3V3_S5 45
PP3V3_S5 72
PP3V3_S5 88 90
HDMI only 32mA?
PP3V3_S5 20
PP3V3_S5 21
PP3V3_S5 113

TBT 3V3 Rails

54 PP3V3_S0_TBT
PP3V3_S0_TBT
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
MAKE_BASE=TRUE
VOLTAGE=3.3V
107
PP3V3_S0_TBT 72
PP3V3_S0_TBT 72

TBT X 3V3 Rails

72 PP3V3_S0SW_TBT_X
PP3V3_S0SW_TBT_X
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
MAKE_BASE=TRUE
VOLTAGE=3.3V
106
PP3V3_S0SW_TBT_X 27

TBT T 3V3 Rails

72 PP3V3_S0SW_TBT_T
PP3V3_S0SW_TBT_T
MIN_LINE_WIDTH=0.1010
MIN_NECK_WIDTH=0.0650
MAKE_BASE=TRUE
VOLTAGE=3.3V
PP3V3_S0SW_TBT_T 93

VCCSTG From Calpe HIO_SW

70 PP1V_S0SW
PP1V_S0SW
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.0V
MAKE_BASE=TRUE
106
PP1V_S0SW 6 8 11 18

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
Power Aliases - 2

Apple Inc.

DRAWING NUMBER 051-02424
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Misc Alias

NC_GPU_THRMTRIP	NC_GPU_THRMTRIP	MAKE_BASE=TRUE
I2C_UPC_X_SDA2	I2C_UPC_X_SDA2	MAKE_BASE=TRUE
I2C_UPC_X_SCL2	I2C_UPC_X_SCL2	MAKE_BASE=TRUE
I2C_UPC_T_SDA2	I2C_UPC_T_SDA2	MAKE_BASE=TRUE
I2C_UPC_T_SCL2	I2C_UPC_T_SCL2	MAKE_BASE=TRUE

TOP Side

PPBUS_HS_CPU

CC203	CC202	CC201	CC200
12PF	3.0PF	12PF	3.0PF
CC231	CC230	CC229	CC228
12PF	3.0PF	12PF	3.0PF
CC227	CC226	CC225	CC224
12PF	3.0PF	12PF	3.0PF

PP1V8_SSD0

CC205	CC204
12PF	3.0PF

PP12V_G3H_VIN_P5V_G3S

CC2A5	CC2A4
12PF	3.0PF

PP3V3_G3H_SSD

CC207	CC206
12PF	3.0PF

PP0V85_ENET

CC289	CC288
12PF	3.0PF

PP12V_G3H_ACDC

CC215	CC214	CC213	CC212
12PF	3.0PF	12PF	3.0PF

PP12V_MAIN

CC223	CC222	CC221	CC220	CC219	CC218	CC217	CC216
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PPVCC_S0_CPU_REG

CC235	CC234	CC233	CC232	CC247	CC246	CC245	CC244
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
CC243	CC242	CC241	CC240	CC239	CC238	CC237	CC236
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PPVCCGT_S0_CPU_REG

CC262	CC257	CC256	CC255	CC254	CC250	CC249	CC248
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
CC263	CC261	CC260	CC259	CC258	CC253	CC252	CC251
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PP1V8_AWAKE

CC269	CC268	CC267	CC266	CC265	CC264
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
CC275	CC274	CC273	CC272	CC271	CC270
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PP3V3_ENET

CC281	CC280	CC279	CC278	CC277	CC276
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PPVIN_ENET_P0V85

CC287	CC286	CC285	CC284	CC283	CC282
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PP5V_G3S_USBC

CC297	CC296	CC295	CC294	CC293	CC292	CC291	CC290
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PP12V_G3H_VIN_P3V3_G3H

CC2A3	CC2A2	CC2A1	CC2A0	CC299	CC298
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

BOTTOM Side

PPVCCIO_S0_CPU

CC2A7	CC2A6
12PF	3.0PF

PPBUS_HS_CPU

CC2B3	CC2B2	CC2B1	CC2B0	CC2A9	CC2A8
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PPVCCGT_S0_CPU_REG

CC2B7	CC2B6	CC2B5	CC2B4
12PF	3.0PF	12PF	3.0PF

PPVCC_S0_CPU_REG

CC2C3	CC2C2	CC2C1	CC2C0	CC2B9	CC2B8
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF

PP1V_PRIM

CC2C9	CC2C8	CC2C7	CC2C6	CC2C5	CC2C4
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
CC2D3	CC2D2	CC2D1	CC2D0		
12PF	3.0PF	12PF	3.0PF		

PP12V_G3H_ACDC

CC2D5	CC2D4
12PF	3.0PF

PP12V_MAIN

CC2D7	CC2D6
12PF	3.0PF

PP0V85_ENET

CC2D8	CC2D9
12PF	3.0PF

PP5V_G3S

CC2E0	CC2E1
12PF	3.0PF

PP12V_G3H_VIN_P5V_G3S

CC2E3	CC2E2
12PF	3.0PF

BOM_COST_GROUP=DESENSE

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Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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PPVDDCPU_AWAKE_SOC	CC303 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC302 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF					
PP0V82_SLPDDR	CC301 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC300 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF					
PP1V8_SSD0_S4E0_AVDD18_PLL	PLACE_NEAR=U8600.L2:3MM	CC305 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC304 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V8_SSD0_S4E2_AVDD18_PLL	PLACE_NEAR=U8800.L2:3MM	CC307 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC306 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V8_SSD0_S4E0_PCI_AVDD_H	PLACE_NEAR=U8600.J6:3MM	CC335 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC334 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V8_SSD0_S4E2_PCI_AVDD_H	PLACE_NEAR=U8800.J6:3MM	CC347 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC346 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP3V3_G3H_SSD	PLACE_NEAR=U9000.B4:3MM	CC315 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC314 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP3V3_ENET	PLACE_NEAR=U9300.14:3MM	CC343 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC342 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF				
PP3V3_ENET_PHY_BIASVDDH	PLACE_NEAR=U9300.37:3MM	CC339 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC338 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF				
PP1V2_ENET_INTREG	PLACE_NEAR=U9300.13:3MM	CC325 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC324 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V2_ENET_PHY_PCIEPLL	PLACE_NEAR=U9300.29:3MM	CC385 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC384 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V1_SLPDDR	CC331 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC332 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF					
PP0V9_SLPDDR	PLACE_NEAR=C4410:3MM	CC329 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC328 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF	PLACE_NEAR=C4411:3MM			
PP1V8_SSD0_S4E1_AVDD18_PLL	PLACE_NEAR=U8600.L2:3MM	PLACE_NEAR=U8700.L2:3MM	CC3A5 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3A4 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP1V8_SSD0_S4E3_AVDD18_PLL	PLACE_NEAR=U8800.L2:3MM	PLACE_NEAR=U8900.L2:3MM	CC389 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC388 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP1V8_SSD0_S4E1_PCI_AVDD_H	PLACE_NEAR=U8600.J6:3MM	PLACE_NEAR=U8700.J6:3MM	CC333 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC308 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP1V8_SSD0_S4E3_PCI_AVDD_H	PLACE_NEAR=U8800.J6:3MM	PLACE_NEAR=U8900.J6:3MM	CC345 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC344 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP0V9_SSD0	PLACE_NEAR=C9025:3MM	CC313 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC312 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	PLACE_NEAR=C9025:3MM			
ENET_XTALVDDH	PLACE_NEAR=U9300.17:3MM	CC341 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC340 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF				
PP3V3_ENET_PHY_AVDDH	PLACE_NEAR=U9300.42:3MM	CC337 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC336 2.7PF +/-0.1PF 25V C0G-CERM 0201 NOSTUFF				
PP1V2_ENET_PHY_AVDDL	PLACE_NEAR=U9300.45:3MM	CC387 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC386 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V2_ENET_PHY_GPHYPLL	PLACE_NEAR=U9300.36:3MM	CC383 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC382 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF				
PP1V8_SSD0	PLACE_NEAR=U8600.P9:3MM PLACE_NEAR=U8600.T5:3MM	PLACE_NEAR=U8700.P9:3MM PLACE_NEAR=U8700.T5:3MM	PLACE_NEAR=U8800.P9:3MM PLACE_NEAR=U8800.T5:3MM	PLACE_NEAR=U8900.P9:3MM PLACE_NEAR=U8900.T5:3MM			
PP2V7_NAND_SSD0	PLACE_NEAR=U8600.R2:3MM PLACE_NEAR=U8600.G4:3MM	PLACE_NEAR=U8700.R2:3MM PLACE_NEAR=U8700.G4:3MM	PLACE_NEAR=U8800.R2:3MM PLACE_NEAR=U8800.G4:3MM	PLACE_NEAR=U8900.R2:3MM PLACE_NEAR=U8900.G4:3MM			
PP0V9_SSD0	PLACE_NEAR=U8600.R4:3MM PLACE_NEAR=U8600.R8:3MM	PLACE_NEAR=U8600.G8:3MM PLACE_NEAR=U8600.J8:3MM					
	PLACE_NEAR=U8700.R4:3MM PLACE_NEAR=U8700.R8:3MM	PLACE_NEAR=U8700.G8:3MM PLACE_NEAR=U8700.J8:3MM					
	PLACE_NEAR=U8800.R4:3MM PLACE_NEAR=U8800.R8:3MM	PLACE_NEAR=U8800.G8:3MM PLACE_NEAR=U8800.J8:3MM					
	PLACE_NEAR=U8900.R4:3MM PLACE_NEAR=U8900.R8:3MM	PLACE_NEAR=U8900.G8:3MM PLACE_NEAR=U8900.J6:3MM					
PPBUS_HS_CPU	PLACE_NEAR=R5420:3MM	CC354 12PF 5% 25V C0G-CERM 0201 NOSTUFF	CC350 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	PLACE_NEAR=R5420:3MM			
PPHV_USBC_XA	PLACE_NEAR=U3100:3MM	CC3E1 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3E2 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	PLACE_NEAR=U3100:3MM			
PPHV_USBC_XB	PLACE_NEAR=U3200:3MM	CC3D8 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3D7 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	PLACE_NEAR=U3200:3MM			
PPHV_USBC_TA	PLACE_NEAR=UB300:3MM	CC310 12PF 5% 25V C0G-CERM 0201 NOSTUFF	CC309 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	PLACE_NEAR=UB300:3MM			
PPHV_USBC_TB	PLACE_NEAR=UB400:3MM	CC3D6 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC311 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	PLACE_NEAR=UB400:3MM			
PP12V_MAIN	CC362 12PF 5% 50V C0G-CERM 0201 NOSTUFF	CC357 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	CC356 12PF 5% 50V C0G-CERM 0201 NOSTUFF	CC355 3PF +/-0.1PF 100V C0G 0201 NOSTUFF			
PP12V_S0_CPUCORE_FLT	CC363 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC361 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	CC360 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC359 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	CC358 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC353 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	CC352 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC351 3PF +/-0.1PF 100V C0G 0201 NOSTUFF
PPVCCIO_S0_CPU_REG	CC3B7 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3B6 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	CC3B5 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3B4 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP12V_G3H_VIN_P5V_G3S	CC349 12PF 5% 50V C0G-CERM 0201 NOSTUFF	CC348 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	CC3A9 12PF 5% 50V C0G-CERM 0201 NOSTUFF	CC3A8 3PF +/-0.1PF 100V C0G 0201 NOSTUFF			
PP1V2_S3	CC3D3 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	CC3D2 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3D1 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3D0 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP5V_G3S	CC3C1 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3C0 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	CC3B9 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3B8 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF			
PP3V3_G3H	PLACE_NEAR=L7610:3MM	PLACE_NEAR=L7610:3MM	CC3C9 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3C8 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	CC3C7 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3C6 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF	CC3C5 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3C4 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF
PPVCC_S0_CPU_REG	CC3C3 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3C2 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF					
PP12V_G3H_VIN_P3V3_G3H	PLACE_NEAR=R5420:3MM	CC3B3 12PF 5% 50V C0G-CERM 0201 NOSTUFF	CC3B2 3PF +/-0.1PF 100V C0G 0201 NOSTUFF	PLACE_NEAR=R5420:3MM			
PPVCIO_S0_CPU	CC3A7 12PF 5% 25V NP0-C0G 0201 NOSTUFF	CC3A6 3.0PF +/-0.1PF 25V NP0-C0G 0201 NOSTUFF					

BOM_COST_GROUP=DESENSE

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PAGE TITLE: Desense CAPs 2

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 123 OF 142

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DFU AND FCT TESTPOINTS placed on top side of MLB, oppsite from CPU.

DFU TEST POINTS <RDAR://31619312>

Possibly useful panda signals

removed SOC_DEBUGPRT_RX/TX

TPC402	DEBUG_JTAG_SOC_TDO	38	113
TPC403	DEBUG_JTAG_SOC_TDI	38	113
TPC404	PP1V8_SLPS2R	84	102
TPC405	SOC_SOCHOT_L	37	71 113
TPC406	I2C_PWR_SDA	38	48
TPC407	I2C_UPC_SCL	38	48
TPC4E9	I2C_UPC_SDA	38	48
TPC4F0	DFUMUX_SEL	113	
TPC4Z5	I2C_PWR_SCL	38	48
TPC401	USB_SOC_P	37	113
TPC431	USB_SOC_N	37	113
TPC440			
TPC439			
TPC4G6			

Other I2C TPs

Possibly useful panda signals

TPC435	I2C_FAN_SCL	48	57
TPC438	I2C_FAN_SDA	48	57

DFU NON-CUSTOMER-FACING USB PORTS

PLACE IN ACCESSIBLE BOARD AREA

SWDL

TPC408	USB3_TEST_D2R_N	OUT	14
TPC409	USB3_TEST_D2R_P	OUT	14
TPC410	USB3_TEST_R2D_N	IN	14
TPC411	USB3_TEST_R2D_P	IN	14
TPC412			
TPC413			
TPC414			
TPC415			
TPC416	USB_TEST_N	BI	14
TPC417	USB_TEST_P	BI	14
TPC418			

DZC400 5.5V-0.28PF 0201-THICKSTNCL; DZC401 5.5V-0.28PF 0201-THICKSTNCL; DZC402 5.5V-0.28PF 0201-THICKSTNCL; DZC403 5.5V-0.28PF 0201-THICKSTNCL; DZC408 5.5V-0.28PF 0201-THICKSTNCL; DZC409 5.5V-0.28PF 0201-THICKSTNCL

NON-CUSTOMER-FACING USB PORTS FOR ETHERNET DONGLE(Bristol OS Testing)

PLACE IN ACCESSIBLE BOARD AREA

Ethenet

TPC422	USB3_ENET_ADAPTOR_D2R_N	OUT	14
TPC423	USB3_ENET_ADAPTOR_D2R_P	OUT	14
TPC424	USB3_ENET_ADAPTOR_R2D_N	IN	14
TPC425	USB3_ENET_ADAPTOR_R2D_P	IN	14
TPC426			
TPC427			
TPC428			
TPC429			
TPC419	USB_ENET_ADAPTOR_N	BI	14
TPC420	USB_ENET_ADAPTOR_P	BI	14
TPC421			

DZC410 5.5V-0.28PF 0201-THICKSTNCL; DZC411 5.5V-0.28PF 0201-THICKSTNCL; DZC412 5.5V-0.28PF 0201-THICKSTNCL; DZC413 5.5V-0.28PF 0201-THICKSTNCL; DZC406 5.5V-0.28PF 0201-THICKSTNCL; DZC407 5.5V-0.28PF 0201-THICKSTNCL

TPC430 — PP5V_G3S — 87 103 106

AUDIO JACK

107 61	AUD_CONN_HP_LEFT	IN	
107 61	AUD_CONN_HP_RIGHT	IN	
107 61	AUD_CONN_RING2	IN	
107 61	AUD_CONN_SLEEVE	IN	
107 61	AUD_CONN_HP_SENSE_L	IN	
107 61	AUD_CONN_HP_SENSE_R	IN	
107 61	AUD_CONN_TIP_SENSE	IN	
107 61	AUD_CONN_SLEEVE_XW	IN	
107 61	AUD_CONN_RING2_XW	IN	

TPC4Z9 — GND_AUDIO_CODEC — 59

DEBUG MOJO

TPC451	PCH_UART_DEBUG_R2D	15	28 113
TPC452	PCH_UART_DEBUG_D2R	15	28 113

removed SMC_DEBUGPRT_RX/TX

TPC453

Soc Access w/o Potassium

TPC454	SOC_USB_VBUS	28	37 113
TPC455	USB_SOC_TYPEC_P	28	113
TPC456	USB_SOC_TYPEC_N	28	113
TPC457	PMU_ACTIVE_READY	29	37 71 108 110
TPC458	SOC_FORCE_DFU	28	37 71 113
TPC459	SOC_DFU_STATUS	29	37
TPC460	UPC_XB_DBG3	28	30
TPC461	UPC_XB_DBG4	28	30
TPC462	SOC_DOCK_CONNECT	29	30 38
TPC463	SOC_SWD_MUX_SEL_PCH	15	
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Power Sequence,status,charging

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TPC469	PP1V2_S3	103	107
TPC470	PPVCC_S0_CPU_REG	102	
TPC471	PP5V_G3S	87	103 106
TPC472	PMU_ONOFF_L	71	100
TPC4L6	CPU_PWRGD	6	13 108
TPC474	PMU_ONOFF_R_L	100	113
TPC475	PM_SLP_S3_L	12	14 26 80 92 106 110
TPC476	PM_SLP_S4_L	12	
TPC477	PM_SLP_S5_L	12	110
TPC478	PM_RSMRST_L	12	18 45 67 88 108 110
TPC479	PPDDRVTT_S0_MEM	103	107
TPC481	PP1V_S3	103	
TPC482	PM_SYSRST_L	12	18 45 108
TPC483	PM_PCH_SYS_PWROK	12	45
TPC484	PM_PCH_PWROK	12	34 45 108
TPC485	PLT_RST_L	12	13 15 20 110
TPC487	PM_SLP_S0_L	12	38 71 100
TPC488	SMC_FIXTURE_MODE_L	38	
TPC489	PP1V8_G3S	59	103
TPC490	PP5V_G3S	87	103 106
TPC491	PP3V3_G3H	102	105
TPC492	PP3V3_G3H_SSD	102	
TPC493	PP3V3_S0SW_TBT_X	103	
TPC4B4	PPVDDCPU_AWAKE_SOC	102	
TPC4B6	PVDDQ_EN	47	71
TPC4B7	PVCCIO_EN	71	73
TPC4B8	PP0V9_SLPDDR	102	
TPC4B9	PP1V1_SLPDDR	102	
TPC4C0	PP1V1_SLPS2R	102	
TPC4C1	PP1V8_AWAKE	102	
TPC4J1	SMC_SYSRST_L	38	45 108
TPC4C4	PP1V8_SLPS2R_PMUVDDGPIO	69	
TPC4C5	P1V1_SLPDDR_SOCFET_EN	70	71
TPC4C6	PMU_CLK32K_WLANBT_R	35	71
TPC4C7	SOC_WDOG	38	71
TPC4C8	PMU_CLK32K_SOC	38	71
TPC4C9	PMU_SYS_ALIVE	37	38 71 79 88
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BOM_COST_GROUP=DEBUG

Power Sequence,status,charging

TPC4D0	P5VG3S_EN	47	71 100
TPC4D1	PP0V8_SLPS2R	102	
TPC4D2	PPVDDCPUSRAM_AWAKE	102	
TPC4D3	P5VG3S_PGOOD	47	71
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TPC4F3	PPVCCSA_S0_CPU_REG	102	
TPC4L0	PPVCCIO_S0_CPU	102	
TPC4F4	PP1V_S0SW	103	
TPC4F5	PP1V2_S0SW	103	
TPC4F6	PP1V_PRIM	103	
TPC4F7	PP1V8_S5	105	
TPC4F8	PP3V0_G3H_RTC	102	
TPC4F9	ALL_SYS_PWRGD	45	71 110
TPC4G0	PCH_RTC_RESET_L	12	71
TPC4G1	PM_THRMTRIP_L	13	20
TPC4G2	PM_PWRBTN_L	12	20
TPC4G3	CPU_PROCHOT_R_L	6	
TPC4G4	PP1V2_ENET	83	86
TPC4I2	PP0V85_ENET	83	87 104
TPC4G7	PP2V1_ENET	83	86
TPC4G8	PP3V3_G3H_ENET	85	102
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TPC4H3	PMU_PVDDMAIN_EN	68	71
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TPC4L2	PP2V7_NAND_SSD0	75	76 77 78 79 105 112
TPC4I0	PP3V3_S5	82	103
TPC4I1	PP0V9_SSD0	75	76 77 78 79 105 112
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Soc Access with Potassium

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TPC4A0	USBC_XB_SBU2	30	31
TPC400	USBC_XA_CC1	29	31
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TPC4A5	PP12V_G3H_ACDC	102	106
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TPC4A7	PP12V_G3H_ACDC	102	106
TPC4A8	PP12V_G3H_ACDC	102	106
TPC4A9	PP12V_G3H_ACDC	102	106
TPC4B1			
TPC4B2			
TPC4B3			
TPC4C2			
TPC4D5			
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TPC434	PP12V_G3H_ACDC	102	106
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FCT TEST POINTS (TOP SIDE OF MLB)

AUDIO

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TPC5A1	TP-P5	SPKRCONN_OUTP	60 107
TPC5A0	TP-P5	SPKRCONN_OUTN	60 107
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TPC510	TP-P5	SPKRCONN_OUTP	60 107
TPC511	TP-P5	SPKRCONN_OUTN	60 107
TPC5A2	TP-P5		
TPC5B8	TP-P5	AUD_CONN_RING_SENSE	61
TPC5B7	TP-P5	AUD_CONN_RING2_XW	61 106
TPC5B6	TP-P5	AUD_CONN_TIP_SENSE	61 106
TPC5B5	TP-P5	AUD_CONN_HP_SENSE_R	61 106
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TPC5B3	TP-P5	AUD_CONN_HP_SENSE_L	61 106
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TPC5A9	TP-P5	AUD_CONN_HP_RIGHT	61 106
TPC5B0	TP-P5	AUD_CONN_RING2	61 106
TPC5B2	TP-P5	AUD_CONN_SLEEVE	61 106
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TPC5K1	TP-P5	AUD_CONN_SLEEVE_XW	61 106

USBC (PLACE NEAR CONNECTOR)

TPC5G4	TP-P5	USBC_XA_SBU1	29 31
TPC5G5	TP-P5	USBC_XA_SBU2	29 31
TPC5G6	TP-P5	USBC_TA_SBU1	95 97
TPC507	TP-P5	USBC_TA_SBU2	95 97
TPC508	TP-P5	USBC_TB_SBU1	96 97
TPC509	TP-P5	USBC_TB_SBU2	96 97
TPC5G7	TP-P5	USBC_XA_CC2	29 31
TPC5G9	TP-P5	PPVBUS_USBC_XA	28 29 31 106 107
TPC5H0	TP-P5	PPVBUS_USBC_XA	28 29 31 106 107
TPC5H1	TP-P5	PPVBUS_USBC_XA	28 29 31 106 107
TPC5H3	TP-P5	PPVBUS_USBC_XB	30 31 107
TPC5H4	TP-P5	PPVBUS_USBC_XB	30 31 107
TPC5I8	TP-P5	PPVBUS_USBC_XB	30 31 107
TPC5J1	TP-P5	PPVBUS_USBC_TA	95 97 107
TPC5J0	TP-P5	PPVBUS_USBC_TA	95 97 107
TPC5J2	TP-P5	PPVBUS_USBC_TA	95 97 107
TPC5J4	TP-P5	PPVBUS_USBC_TB	96 97 107
TPC5H5	TP-P5	PPVBUS_USBC_TB	96 97 107
TPC5H6	TP-P5	PPVBUS_USBC_TB	96 97 107
TPC5H7	TP-P5		
TPC5H8	TP-P5		
TPC5M2	TP-P5		
TPC5K2	TP-P5		
TPC5K3	TP-P5		
TPC5K4	TP-P5		
TPC5J5	TP-P5		
TPC5J6	TP-P5		
TPC5N9	TP-P5	USBC_XB_CC1	30 31
TPC5N8	TP-P5	USBC_XB_CC2	30 31
TPC5O1	TP-P5	USBC_TA_CC1	95 97
TPC5O2	TP-P5	USBC_TA_CC2	95 97
TPC5O3	TP-P5	USBC_TB_CC1	96 97
TPC5O4	TP-P5	USBC_TB_CC2	96 97

MISC

TPC540	TP-P5	SYS_LED_DR	100
TPC541	TP-P5	ISNS_P1V2_N	52 67
TPC542	TP-P5	ISNS_P1V2_P	52 67
TPC543	TP-P5	ISNS_P3V3_G3H_HI_N	51
TPC544	TP-P5	ISNS_P3V3_G3H_HI_P	51
TPC545	TP-P5	ISNS_P3V3_WLANBT_N	56
TPC548	TP-P5	ISNS_P3V3_WLANBT_P	56
TPC547	TP-P5	ISNS_P5V_G3S_HI_N	51
TPC546	TP-P5	ISNS_P5V_G3S_HI_P	51
TPC549	TP-P5	ISNS_PMU_N	54
TPC512	TP-P5	ISNS_PMU_P	54
TPC551	TP-P5	PMU_P3V3_CAPLE_ISENSE	46 54
TPC552	TP-P5	PP12V_FAN_FET	57
TPC513	TP-P5	PP12V_G3H_VIN_P3V3_G3H	102
TPC515	TP-P5	PP12V_G3H_VIN_P5V_G3S	102
TPC514	TP-P5	PP12V_S0_CPUCORE_FLT	51 63 105
TPC518	TP-P5	PP2V5_S3_VPP	103
TPC517	TP-P5	PP3V3_G3H_PMU	102
TPC516	TP-P5	PP3V3_S0_TBT	103
TPC519	TP-P5	PP5V_G3S_USBA	103
TPC523	TP-P5	PP5V_G3S_USBC	28 94 103
TPC522	TP-P5	PPBUS_HS_CPU	102
TPC520	TP-P5	PPCPUVCCSA_S0_SENSE_1	66
TPC521	TP-P5	PPVCCIO_S0_CPU_REG	54 73 105
TPC524	TP-P5	PPVDDQ_S3_REG_R	67
TPC527	TP-P5	PPVIN_ENET_P0V85	102
TPC526	TP-P5	PPVIN_G3H_P2V7	102
TPC525	TP-P5	SMC_CPU_HI_ISENSE	46 51
TPC528	TP-P5	SMC_CPU_VCC_ISENSE	46 52
TPC529	TP-P5	SMC_CPUGT_ISENSE	46 54
TPC530	TP-P5	SMC_P12VIN_ISENSE	46 51
TPC531	TP-P5	SMC_P1V2_ISENSE	46 52
TPC534	TP-P5	XDP_CPU_TCK	6 18 108
TPC533	TP-P5	XDP_CPU_TDI	6 18 108
TPC532	TP-P5	XDP_CPU_TDO	6 18 108
TPC535	TP-P5	XDP_CPU_TMS	6 18 108
TPC536	TP-P5	XDP_CPU_TRST_L	6 13 18 108

HDMI Test Poins

TPC556	TP-P5	HDMI_CEC_CONN	88
TPC557	TP-P5	HDMI_RSVD	88
TPC561	TP-P5	HDMI_DDC_5V_CONN_SCL	88
TPC563	TP-P5	HDMI_DDC_5V_CONN_SDA	88
TPC5Y9	TP-P5	HDMI_HPD_IN_CONN	88
TPC592	TP-P5	PP5V0_HDMI_DDC_CONN	88
TPC593	TP-P5		
TPC594	TP-P5		

FAN Test Points

TPC558	TP-P5	FAN_0_PWM_FILT	57
TPC559	TP-P5	FAN_0_TACH_FILT	57
TPC562	TP-P5	PP12V_FAN_FILT	57
TPC564	TP-P5		
TPC565	TP-P5		

WIRELESS

TPC5H9	TP-P5	PP3V3_G3S_WLANBT	35 103
TPC5I0	TP-P5	PP1V8_G3S	34 35 103
TPC5L0	TP-P5	PPVIN_RFLDO_WLANBT	35
TPC5L1	TP-P5	PP1V2_WLANBT	35
TPC5L2	TP-P5	PP1V5_WLANBT	35

USB-A Test Poins

High Speed - Tear drops, NO TP

62	IN	USB3_EXTA_TX_F_P
62	IN	USB3_EXTA_TX_F_N
62	IN	USB3_EXTA_RX_P
62	IN	USB3_EXTA_RX_N
62	IN	USB2_EXTA_P
62	IN	USB2_EXTA_N
62	IN	USB3_EXTB_TX_F_P
62	IN	USB3_EXTB_TX_F_N
62	IN	USB3_EXTB_RX_P
62	IN	USB3_EXTB_RX_N
62	IN	USB2_EXTB_P
62	IN	USB2_EXTB_N

TPC595	TP-P5	PP5V_S4_EXTA_F	62 107
TPC596	TP-P5	PP5V_S4_EXTB_F	62 107
TPC599	TP-P5		
TPC5A6	TP-P5		
TPC5C5	TP-P5	PP5V_S4_EXTA_F	62 107
TPC5C6	TP-P5	PP5V_S4_EXTB_F	62 107
TPC5C7	TP-P5		
TPC5C8	TP-P5		

ENET HS signals - Tear drops, NO TP

109 85	IN	ENET_CONN_A_P
109 85	IN	ENET_CONN_A_N
109 85	IN	ENET_CONN_B_P
109 85	IN	ENET_CONN_B_N
109 85	IN	ENET_CONN_C_P
109 85	IN	ENET_CONN_C_N
109 85	IN	ENET_CONN_D_P
109 85	IN	ENET_CONN_D_N

MEMORY

TPC5I3	TP-P5	PVDDQ_PGOOD	47 71 110
TPC5I4	TP-P5	PP1V2_S3	103 106 107
TPC5I5	TP-P5	PP2V5_S3	103
TPC5I6	TP-P5	PPDDRVTT_S0_MEM	103 106
TPC5I7	TP-P5	PP1V2_S3	103 106 107

PSU Test Points

TPC501	TP-P5	SNS_ACDC_P	55 100
TPC500	TP-P5	SNS_ACDC_N	55 100
TPC503	TP-P5	ACDC_ID	100
TPC504	TP-P5	ACDC_BURST_EN_L	100
TPC502	TP-P5	SYS_LED	46 100

HDMI

TPC505	TP-P5	DDI2_MUX_SEL	21 28
TPC506	TP-P5	DDI1_MUX_SEL	21 28

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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ICT TEST POINTS, ICT BOUNDARY SCAN TESTPOINTS

CPU XDP and PCH Test-Points

107 18 6	IN	XDP_CPU_TCK
18 13	IN	XDP_PCH_TCK
107 18 6	IN	XDP_CPU_TDI
107 18 6	IN	XDP_CPU_TDO
107 18 13 6	IN	XDP_CPU_TRST_L
107 18 6	IN	XDP_CPU_TMS
18 13	IN	XDP_PCH_TMS
18 13	IN	XDP_PCH_TDI
18 13	IN	XDP_PCH_TDO
18 13 6	IN	XDP_CPU_PREQ_L
18 13 6	IN	XDP_CPU_PRDY_L
47 45 18 13 110 106	IN	PM_RSMRST_L
106 45 34 12	IN	PM_PCH_PWROK
106 45 18 12	IN	PM_SYSRST_L
18 6	IN	CPU_CFG<3>
18 13	IN	PCH_JTAGX
18 13	BI	PCH_ITP_PMODE

H9M BOUNDARY SCAN TESTPOINTS ON FCT TESTPOINT PAGE

OTHER ICT TESTPONTS

ACE

26 15	BI	JTAG_TBT_X_TMS
94 92 26	BI	JTAG_ISP_TDI
94 92 26	BI	JTAG_ISP_TCK
94 92 26	BI	JTAG_ISP_TDO
108 26	BI	TBT_X_TEST_EN

WLAN

38 36	BI	WLAN_JTAG_TMS
38 36	BI	WLAN_JTAG_TCK
39 36	BI	WLAN_JTAG_TDI
36 35	BI	WLAN_JTAG_TDO
36 35	BI	WLAN_JTAG_TRST_L
92 15	BI	JTAG_TBT_T_TMS
38	BI	TP_JTAG_SOC_TRST_L
45 38	BI	SMC_PCH_SYS_PWROK
45 38	BI	SMC_PCH_PWROK
106 45 38	BI	SMC_SYSRST_L
106 13 6	BI	CPU_PWRGD
106 71 38	BI	PMU_COLD_RESET_L
38	BI	SOC_JTAG_SEL
37	BI	SOC_TESTMODE
36 35	BI	WLAN_JTAG_SEL
92	BI	TBT_T_TEST_EN
108 26	BI	TBT_X_TEST_EN

TP of HDMI (EE tests)

TPC646	DP2HDMI_PMU_CEC_IRQ	90
TPC641	DP2HDMI_1.5G_FILT_EN	88 90

TP of Calpe PMIC (EE tests)

TPC642	TP_PP1V8_PMU_BUCK3SW5	69
TPC643	TP_PP1V1_PMU_BUCK4SW1	69
TPC644	TP_PP1V2_PMU_BUCK6SW1	69 108
TPC645	TP_PP1V_PMU_BUCK8SW1	69 108
TPC676	SOC_VDDCPU_SENSE	41 71
TPC664	TP_P3V3G3W_EN	71
TPC665	TP_P3V3G3W_PGOOD	71
TPC667	TP_SE_PWR_EN	71
TPC668	TP_P3V3_S5_EN	71
TPC670	TP_PVCCEOPIOEDRAM_P2V7NAND_PGOOD	
TPC671	TP_PEARL_P2V7NAND_EN	71
TPC672	TP_NAND_DISCHARGE_HDD_PWR_EN	71
TPC673	TP_NAND_RESET_L_SD_PWR_EN	71
TPC674	ENET_PWR_EN	71 72 85 86 87
TPC675	TBT_PWR_EN	71 72
TPC679	UPC_TA_GPIO7	95
TPC635	BT_PWR_EN	35 36 71
TPC669	WLAN_PWR_EN	35 36 71
TPC680	UPC_TB_GPIO7	96
TPC681	TP_PP1V2_PMU_BUCK6SW1	69 108
TPC682	TP_PP1V_PMU_BUCK8SW1	69 108
TPC677	FAN_PWR_EN	57 71
TPC683	PVCCIO_PGOOD	47 71
TPC684	P3V3MAIN_PGOOD	47 71 110
TPC636	PVCCPLLOC_EN	71 72

Test Points for Calpe breakout

TPC647	PMU_VCCIO_ISENSE	46 71 108
TPC648	PMU_VCCIO_ISENSE	46 71 108
TPC649	PMU_VCCIO_ISENSE	46 71 108
TPC650	PMU_P5V_G3S_HI_ISENSE	46 71
TPC651	PMU_CPUSA_VSENSE	46 71
TPC652	PMU_P5V_USBC_ISENSE	46 71
TPC653	PMU_P5V_USBA_ISENSE	46 71
TPC654	TP_PMU_AMUX_AY	71
TPC655	PMU_P3V3_TBT_ISENSE	46 71
TPC656	PMU_P3V3_SSD0_ISENSE	46 71
TPC657	PMU_PBUS_SSD0_ISENSE	46 71
TPC658	PMU_P3V3_G3H_HI_ISENSE	46 71
TPC659	PMU_P3V3_WLANBT_ISENSE	46 71
TPC660	PMU_P3V3_ENET_ISENSE	46 71
TPC661	PMU_P12V_ENET_ISENSE	46 71
TPC662	TP_PMU_AMUX_B7	71
TPC663	TP_PMU_AMUX_BY	71

TP of H9ML (EE tests)

TPC678	PCC_EVENT	38
TPC686	TP_SMC_DEBUG	46
TPC687	WLAN_CONTEXT_A	35 36 38
TPC688	WLAN_CONTEXT_B	35 36 38

TP of CONTEXT_A/B can be used for AOP_UART_TX/RX for debug

TPC600	LIDOPEN_PSU12VPGOOD_ACDCBURST_L	38 100
TPC6G8	SWD_SOC_SWDIO	38 46 113
TPC6G9	SWD_SOC_SWCLK	38 46 113

EE TESTS PCH

TPC631	PCIE_CLK100M_WLAN_PCH_N	12 20
TPC632	PCIE_CLK100M_WLAN_PCH_P	12 20
TPC633	PCIE_CLK100M_SOC_N	12 40
TPC634	PCIE_CLK100M_SOC_P	12 40
TPC637	PCIE_CLK100M_TBT_X_N	12 26
TPC638	PCIE_CLK100M_TBT_X_P	12 26
TPC639	PCIE_CLK100M_TBT_T_N	12 92
TPC640	PCIE_CLK100M_TBT_T_P	12 92
TPC690	SPI_PCHROM_MOSI	13 18
TPC691	TP_PCH_CLK32K_SUS	12
TPC692	SPI_IO<2>	13 18
TPC693	SPI_IO<3>	13

TP Debug ACE Nets (EE tests)

TPC622	UPC_XA_DEBUGUART_TX	29
TPC623	PMU_ACTIVE_READY	29 37 71 106 110
TPC624	UPC_XB_DEBUGUART_TX	30
TPC625	UPC_XB_GPIO1	30

Test Points for Ace XA/XB GPIO0/1, must have in production.

TPC626	UPC_TA_DEBUGUART_TX	95
TPC627	UPC_TA_GPIO1	95
TPC628	UPC_TB_DEBUGUART_TX	96
TPC629	UPC_TB_GPIO1	96

Test Points for Ace XA/XB GPIO0/1, must have in production.

SENSOR TPs

TPC694	SNS_P12VG3H_P	51
TPC695	SNS_P12VG3H_N	51
TPC6C9	ISNS_HS_COMPUTING_P	51
TPC6C8	ISNS_HS_COMPUTING_N	51
TPC6D2	CPUVR_ISNS_R_P	52
TPC6D1	CPUVR_ISNS_R_N	52
TPC6D0	ISNS_P3V3_G3W_SSD0_P	53
TPC6D3	ISNS_P3V3_G3W_SSD0_N	53
TPC6D6	ISNS_PPBUS_MAIN_SSD0_P	53
TPC6D5	ISNS_PPBUS_MAIN_SSD0_N	53
TPC6D4	ISNS_TBT_P	54
TPC6D8	ISNS_TBT_N	54
TPC6D7	ISNS_CPUVCCIO_P	54
TPC6E0	ISNS_CPUVCCIO_N	54
TPC6E1	CPUGT_ISNS_P	54
TPC6D9	CPUGT_ISNS_N	54
TPC6E4	ISNS_P5V_USBC_P	56
TPC6E3	ISNS_P5V_USBC_N	56
TPC6E2	ISNS_P5V_USBA_P	56
TPC6E6	ISNS_P5V_USBA_N	56
TPC6E5	ISNS_P3V3_ENET_P	56
TPC6E8	ISNS_P3V3_ENET_N	56
TPC6E9	ISNS_P12V_ENET_P	56
TPC6E7	ISNS_P12V_ENET_N	56
TPC6F0	PMU_CPUSA_VSENSE	46 56
TPC6F1	SMC_CPU_VCC_VSENSE	46 56
TPC6F4	SMC_CPUGT_VSENSE	46 56
TPC6F2	TSNS_T1_DX1_P	55
TPC6F3	TSNS_T1_DX2_P	55
TPC6F6	TSNS_T1_DX3_P	55
TPC6F7	TSNS_T1_DX4_P	55
TPC6F5	TSNS_T1_DX5_P	55
TPC6F9	TSNS_T1_DX6_P	55
TPC6F8	TSNS_T1_DX7_P	55
TPC6G0	TSNS_T1_DX8_P	55
TPC6G1	TSNS_T1_DN	55
TPC6G2	TSNS_T2_DX1_P	55
TPC6G4	TSNS_T2_DX4_P	55
TPC6G3	TSNS_T2_DX4_N	55
TPC6G5	TSNS_T2_DN	55
TPC6G6	TBTTHMSNS_X_D2_P	55
TPC6G7	TBTTHMSNS_X_D2_N	55
TPC6H1	REG_VCCSA_ISNS_1_P	54 66
TPC6H0	REG_VCCSA_ISNS_1_N	54 66
TPC6H3	ISNS_2V5_S3_P	52
TPC6H2	ISNS_2V5_S3_N	52
TPC6H5	TBTTHMSNS_T_D3_P	55
TPC6H4	TBTTHMSNS_T_D3_N	55

S4E

TPC619	SSD0_CLKREQ0_L	40 46 75
TPC617	SSD0_CLKREQ1_L	40 46 76
TPC616	SSD0_CLKREQ2_L	40 46 77
TPC630	SSD0_CLKREQ3_L	40 46 78
TPC614	SSD0_S4E0_DROOP_L	75
TPC618	SSD0_S4E1_DROOP_L	76
TPC611	SSD0_S4E2_DROOP_L	77
TPC612	SSD0_S4E3_DROOP_L	78
TPC685	SSD0_OCARINA_VDD_LDO	79
TPC689	SSD0_OCARINA_WP_L	75 76 77 78 79
TPC601	SSD0_VR_P2V7_EN	79
TPC602	SSD0_OCARINA_RESET_L	75 76 77 78 79
TPC603	SSD0_VR_P2V7_PGOOD	79
TPC604	SSD0_OCARINA_TCAL	79
TPC606	SSD0_OCARINA_PFN	75 76 77 78 79
TPC605	SSD0_OCARINA_FORCE_EN	79
TPC607	SSD0_OCARINA_VREF	79
TPC608	SSD0_S4E_BOOT2	74 75 76 77 78
TPC609	SSD0_S4E0_ZQ_C	75
TPC615	SSD0_S4E0_ZQ_L	75
TPC610	SSD0_S4E1_ZQ_C	76
TPC613	SSD0_S4E1_ZQ_L	76
TPC620	SSD0_S4E2_ZQ_C	77
TPC666	SSD0_S4E2_ZQ_L	77
TPC621	SSD0_S4E3_ZQ_C	78
TPC696	SSD0_S4E3_ZQ_L	78
TPC697	SSD0_S4E0_PCIE_RESREF	75
TPC698	SSD0_S4E1_PCIE_RESREF	76
TPC6A1	SSD0_S4E2_PCIE_RESREF	77
TPC6A0	SSD0_S4E3_PCIE_RESREF	78
TPC699	I2C_SSD_SCL	38 48
TPC6A2	I2C_SSD_SDA	38 48
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SSD BOUNDARY SCAN Test-Points

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TPC6B5	TP_SSD0_S4E1_ANI0_VREF	76
TPC6B4	TP_SSD0_S4E2_ANI1_VREF	77
TPC6B7	TP_SSD0_S4E2_ANI0_VREF	77
TPC6B8	TP_SSD0_S4E3_ANI1_VREF	78
TPC6B9	TP_SSD0_S4E3_ANI0_VREF	78
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TPC6C0	SSD0_S4E0_SWD_UID1	75
TPC6C2	SSD0_S4E1_SWD_UID0	76
TPC6C3	SSD0_S4E1_SWD_UID1	76
TPC6C4	SSD0_S4E2_SWD_UID0	77
TPC6C6	SSD0_S4E2_SWD_UID1	77
TPC6C7	SSD0_S4E3_SWD_UID0	78
TPC6C5	SSD0_S4E3_SWD_UID1	78

BOM_COST_GROUP=PCB

PAGE TITLE: ICT, MAC-1 ,EE Testpoints

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

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ICT TESTPOINTS , High Speed NO_TEST

CPU

PEG

84 5	PCIE ENET D2R N<3..0>	NO_TEST=1
84 5	PCIE ENET D2R P<3..0>	NO_TEST=1
84 5	PCIE ENET R2D C N<3..0>	NO_TEST=1
84 5	PCIE ENET R2D C P<3..0>	NO_TEST=1
94 5	PCIE TBT T D2R N<3..0>	NO_TEST=1
94 5	PCIE TBT T D2R P<3..0>	NO_TEST=1
94 5	PCIE TBT T R2D C N<3..0>	NO_TEST=1
94 5	PCIE TBT T R2D C P<3..0>	NO_TEST=1
26 5	PCIE TBT X D2R N<3..0>	NO_TEST=1
28 5	PCIE TBT X D2R P<3..0>	NO_TEST=1
28 5	PCIE TBT X R2D C N<3..0>	NO_TEST=1
28 5	PCIE TBT X R2D C P<3..0>	NO_TEST=1

DMI

13 5	DMI S2N N<3..0>	NO_TEST=1
13 5	DMI S2N P<3..0>	NO_TEST=1
13 5	DMI N2S N<3..0>	NO_TEST=1
13 5	DMI N2S P<3..0>	NO_TEST=1

DDI

21 5	DP DDI1 ML C N<3..0>	NO_TEST=1
21 5	DP DDI1 ML C P<3..0>	NO_TEST=1
21 5	DP DDI2 ML C N<3..0>	NO_TEST=1
21 5	DP DDI2 ML C P<3..0>	NO_TEST=1
91 5	DP DDI3 ML C N<3..0>	NO_TEST=1
91 5	DP DDI3 ML C P<3..0>	NO_TEST=1
21 5	DP DDI1 AUXCH C N	NO_TEST=1
21 5	DP DDI1 AUXCH C P	NO_TEST=1
21 5	DP DDI2 AUXCH C N	NO_TEST=1
21 5	DP DDI2 AUXCH C P	NO_TEST=1
91 5	DP DDI3 AUXCH C N	NO_TEST=1
91 5	DP DDI3 AUXCH C P	NO_TEST=1

CPU CLK

12 6	CPU CLK24M NSSC CLK N	NO_TEST=1
12 6	CPU CLK24M NSSC CLK P	NO_TEST=1
12 6	CPU CLK100M PCIBCLK N	NO_TEST=1
12 6	CPU CLK100M PCIBCLK P	NO_TEST=1
12 6	CPU CLK100M BCLK N	NO_TEST=1
12 6	CPU CLK100M BCLK P	NO_TEST=1

DDR4 MEM

25 7	MEM A DQ<63..0>	NO_TEST=1
25 7	MEM A DQS N<7..0>	NO_TEST=1
25 7	MEM A DQS P<7..0>	NO_TEST=1
23 7	MEM A CLK N<1..0>	NO_TEST=1
23 7	MEM A CLK P<1..0>	NO_TEST=1
23 7	MEM A CKE<1..0>	NO_TEST=1
23 7	MEM A CS L<1..0>	NO_TEST=1
23 7	MEM A ODT<1..0>	NO_TEST=1
23 7	MEM A BA<1..0>	NO_TEST=1
23 7	MEM A BG<1..0>	NO_TEST=1
23 7	MEM A ACT L	NO_TEST=1
23 7	MEM A ALERT L	NO_TEST=1
23 7	MEM A PAR	NO_TEST=1
23 7	MEM A A<16..0>	NO_TEST=1
25 7	MEM B DQ<63..0>	NO_TEST=1
25 7	MEM B DQS N<7..0>	NO_TEST=1
25 7	MEM B DQS P<7..0>	NO_TEST=1
24 7	MEM B CLK N<1..0>	NO_TEST=1
24 7	MEM B CLK P<1..0>	NO_TEST=1
24 7	MEM B CKE<1..0>	NO_TEST=1
24 7	MEM B CS L<1..0>	NO_TEST=1
24 7	MEM B ODT<1..0>	NO_TEST=1
24 7	MEM B BA<1..0>	NO_TEST=1
24 7	MEM B BG<1..0>	NO_TEST=1
24 7	MEM B ACT L	NO_TEST=1
24 7	MEM B ALERT L	NO_TEST=1
24 7	MEM B PAR	NO_TEST=1
24 7	MEM B A<16..0>	NO_TEST=1

PMIC

XTAL

71	PMU XTAL1	NO_TEST=1
71	PMU XTAL1 R	NO_TEST=1
71	PMU XTAL2	NO_TEST=1

PCH

CLK

18 12	ITPXDP CLK100M N	NO_TEST=1
18 12	ITPXDP CLK100M P	NO_TEST=1

USB 3.0

113 109 14	USB3 VITAMIN D2R N	NO_TEST=1
113 109 14	USB3 VITAMIN D2R P	NO_TEST=1
113 109 14	USB3 VITAMIN D2R N	NO_TEST=1
113 109 14	USB3 VITAMIN D2R P	NO_TEST=1
113 14	USB3 VITAMIN R2D C N	NO_TEST=1
113 14	USB3 VITAMIN R2D C P	NO_TEST=1
62 14	USB3 EXTA D2R N	NO_TEST=1
62 14	USB3 EXTA D2R P	NO_TEST=1
62 14	USB3 EXTA R2D C N	NO_TEST=1
62 14	USB3 EXTA R2D C P	NO_TEST=1
62 14	USB3 EXTB D2R N	NO_TEST=1
62 14	USB3 EXTB D2R P	NO_TEST=1
62 14	USB3 EXTB R2D C N	NO_TEST=1
62 14	USB3 EXTB R2D C P	NO_TEST=1

PCIE

20 14	PCIE WLANPCH D2R N	NO_TEST=1
20 14	PCIE WLANPCH D2R P	NO_TEST=1
20 14	PCIE WLANPCH R2D C N	NO_TEST=1
20 14	PCIE WLANPCH R2D C P	NO_TEST=1
81 14	PCIE ENET PCH D2R N	NO_TEST=1
81 14	PCIE ENET PCH D2R P	NO_TEST=1
81 14	PCIE ENET PCH R2D C N	NO_TEST=1
81 14	PCIE ENET PCH R2D C P	NO_TEST=1
40 14	PCIE SOC D2R N<3..0>	NO_TEST=1
40 14	PCIE SOC D2R P<3..0>	NO_TEST=1
46 14	PCIE SOC R2D C N<3..0>	NO_TEST=1
46 14	PCIE SOC R2D C P<3..0>	NO_TEST=1

PCIE

19	PCH CLK24M XTALOUT R	NO_TEST=1
19 12	PCH CLK24M XTALIN	NO_TEST=1
19 12	PCH CLK24M XTALOUT	NO_TEST=1

Display MUX

DP

92 21	DP T SNK1 ML C N<3..0>	NO_TEST=1
92 21	DP T SNK1 ML C P<3..0>	NO_TEST=1
92 21	DP T SNK0 ML C N<3..0>	NO_TEST=1
92 21	DP T SNK0 ML C P<3..0>	NO_TEST=1
92 21	DP T SNK1 AUXCH C N	NO_TEST=1
92 21	DP T SNK1 AUXCH C P	NO_TEST=1
92 21	DP T SNK0 AUXCH C N	NO_TEST=1
92 21	DP T SNK0 AUXCH C P	NO_TEST=1
26 21	DP X SNK1 ML C N<3..0>	NO_TEST=1
26 21	DP X SNK1 ML C P<3..0>	NO_TEST=1
26 21	DP X SNK0 ML C N<3..0>	NO_TEST=1
26 21	DP X SNK0 ML C P<3..0>	NO_TEST=1
26 21	DP X SNK1 AUXCH C N	NO_TEST=1
26 21	DP X SNK1 AUXCH C P	NO_TEST=1
26 21	DP X SNK0 AUXCH C N	NO_TEST=1
26 21	DP X SNK0 AUXCH C P	NO_TEST=1

SSD

PCIE

78 77 76 75	PCIE SSD0 D2R C N<3..0>	NO_TEST=1
78 77 76 75	PCIE SSD0 D2R C P<3..0>	NO_TEST=1
78 77 76 75	PCIE SSD0 R2D N<3..0>	NO_TEST=1
78 77 76 75	PCIE SSD0 R2D P<3..0>	NO_TEST=1

Titan Ridges

PCIE

28 26	PCIE TBT X R2D N<3..0>	NO_TEST=1
28 26	PCIE TBT X R2D P<3..0>	NO_TEST=1
28 26	PCIE TBT X D2R C N<3..0>	NO_TEST=1
28 26	PCIE TBT X D2R C P<3..0>	NO_TEST=1
94 92	PCIE TBT T R2D N<3..0>	NO_TEST=1
94 92	PCIE TBT T R2D P<3..0>	NO_TEST=1
94 92	PCIE TBT T D2R C N<3..0>	NO_TEST=1
94 92	PCIE TBT T D2R C P<3..0>	NO_TEST=1

DP

26	DP X SNK0 ML N<3..0>	NO_TEST=1
26	DP X SNK0 ML P<3..0>	NO_TEST=1
26	DP X SNK0 AUXCH N	NO_TEST=1
26	DP X SNK0 AUXCH P	NO_TEST=1
26	DP X SNK1 ML N<3..0>	NO_TEST=1
26	DP X SNK1 ML P<3..0>	NO_TEST=1
26	DP X SNK1 AUXCH N	NO_TEST=1
26	DP X SNK1 AUXCH P	NO_TEST=1
92	DP T SNK0 ML N<3..0>	NO_TEST=1
92	DP T SNK0 ML P<3..0>	NO_TEST=1
92	DP T SNK0 AUXCH N	NO_TEST=1
92	DP T SNK0 AUXCH P	NO_TEST=1
92	DP T SNK1 ML N<3..0>	NO_TEST=1
92	DP T SNK1 ML P<3..0>	NO_TEST=1
92	DP T SNK1 AUXCH N	NO_TEST=1
92	DP T SNK1 AUXCH P	NO_TEST=1

USB-C

31 26	USBC XA D2R N<2..1>	NO_TEST=1
31 26	USBC XA D2R P<2..1>	NO_TEST=1
31 26	USBC XA R2D C N<2..1>	NO_TEST=1
31 26	USBC XA R2D C P<2..1>	NO_TEST=1
31 26	USBC XB D2R N<2..1>	NO_TEST=1
31 26	USBC XB D2R P<2..1>	NO_TEST=1
31 26	USBC XB R2D C N<2..1>	NO_TEST=1
31 26	USBC XB R2D C P<2..1>	NO_TEST=1
97 92	USBC TA D2R N<2..1>	NO_TEST=1
97 92	USBC TA D2R P<2..1>	NO_TEST=1
97 92	USBC TA R2D C N<2..1>	NO_TEST=1
97 92	USBC TA R2D C P<2..1>	NO_TEST=1
97 92	USBC TB D2R N<2..1>	NO_TEST=1
97 92	USBC TB D2R P<2..1>	NO_TEST=1
97 92	USBC TB R2D C N<2..1>	NO_TEST=1
97 92	USBC TB R2D C P<2..1>	NO_TEST=1

XTAL

28 26	TBT X XTAL25M OUT	NO_TEST=1
28 26	TBT X XTAL25M IN	NO_TEST=1
28	TBT X XTAL25M OUT R	NO_TEST=1

Madea

DP

91 90	LPDPTX DATA N<3..0>	NO_TEST=1
91 90	LPDPTX DATA P<3..0>	NO_TEST=1
91 90	LPDPTX AUX N	NO_TEST=1
91 90	LPDPTX AUX P	NO_TEST=1

HDMI

90 89	HDMI DATA N<2..0>	NO_TEST=1
90 89	HDMI DATA P<2..0>	NO_TEST=1
89 88	HDMI DATA CONN N<2..0>	NO_TEST=1
89 88	HDMI DATA CONN P<2..0>	NO_TEST=1
89 88	HDMI CLK CONN N	NO_TEST=1
89 88	HDMI CLK CONN P	NO_TEST=1
89	HDMI CLK FLT N	NO_TEST=1
89	HDMI CLK FLT P	NO_TEST=1
89	HDMI CLK R N	NO_TEST=1
89	HDMI CLK R P	NO_TEST=1
90 89	HDMI CLK N	NO_TEST=1
90 89	HDMI CLK P	NO_TEST=1

USB-C CONN

USB-C

31	USBC XA D2R RC N<2..1>	NO_TEST=1
31	USBC XA D2R RC P<2..1>	NO_TEST=1
31	USBC XA R2D RC N<2..1>	NO_TEST=1
31	USBC XA R2D RC P<2..1>	NO_TEST=1
31	USBC XA D2R CONN N<2..1>	NO_TEST=1
31	USBC XA D2R CONN P<2..1>	NO_TEST=1
31	USBC XA R2D CONN N<2..1>	NO_TEST=1
31	USBC XA R2D CONN P<2..1>	NO_TEST=1
31 28	USBC XA USB DBG TOP N	NO_TEST=1
31 28	USBC XA USB DBG TOP P	NO_TEST=1
31 28	USBC XA USB DBG BOT N	NO_TEST=1
31 28	USBC XA USB DBG BOT P	NO_TEST=1
31	USBC XB D2R RC N<2..1>	NO_TEST=1
31	USBC XB D2R RC P<2..1>	NO_TEST=1
31	USBC XB R2D RC N<2..1>	NO_TEST=1
31	USBC XB R2D RC P<2..1>	NO_TEST=1
31	USBC XB D2R CONN N<2..1>	NO_TEST=1
31	USBC XB D2R CONN P<2..1>	NO_TEST=1
31	USBC XB R2D CONN N<2..1>	NO_TEST=1
31	USBC XB R2D CONN P<2..1>	NO_TEST=1
31 30	USBC XB USB TOP N	NO_TEST=1
31 30	USBC XB USB TOP P	NO_TEST=1
31 30	USBC XB USB BOT N	NO_TEST=1
31 30	USBC XB USB BOT P	NO_TEST=1
97	USBC TA D2R RC N<2..1>	NO_TEST=1
97	USBC TA D2R RC P<2..1>	NO_TEST=1
97	USBC TA R2D RC N<2..1>	NO_TEST=1
97	USBC TA R2D RC P<2..1>	NO_TEST=1
97	USBC TA D2R CONN N<2..1>	NO_TEST=1
97	USBC TA D2R CONN P<2..1>	NO_TEST=1
97	USBC TA R2D CONN N<2..1>	NO_TEST=1
97	USBC TA R2D CONN P<2..1>	NO_TEST=1
97 95	USBC TA USB TOP N	NO_TEST=1
97 95	USBC TA USB TOP P	NO_TEST=1
97 95	USBC TA USB BOT N	NO_TEST=1
97 95	USBC TA USB BOT P	NO_TEST=1
97	USBC TB D2R RC N<2..1>	NO_TEST=1
97	USBC TB D2R RC P<2..1>	NO_TEST=1
97	USBC TB R2D RC N<2..1>	NO_TEST=1
97	USBC TB R2D RC P<2..1>	NO_TEST=1
97	USBC TB D2R CONN N<2..1>	NO_TEST=1
97	USBC TB D2R CONN P<2..1>	NO_TEST=1
97	USBC TB R2D CONN N<2..1>	NO_TEST=1
97	USBC TB R2D CONN P<2..1>	NO_TEST=1
97 96	USBC TB USB TOP N	NO_TEST=1
97 96	USBC TB USB TOP P	NO_TEST=1
97 96	USBC TB USB BOT N	NO_TEST=1
97 96	USBC TB USB BOT P	NO_TEST=1

Harpoon

ANT MATCH

36 35	50 G 0 MATCH	NO_TEST=1
36 35	50 A 0 MATCH	NO_TEST=1
36 35	50 G 1 MATCH	NO_TEST=1
36 35	50 A 1 MATCH	NO_TEST=1
36 35	50 G 2 MATCH	NO_TEST=1
36 35	50 A 2 MATCH	NO_TEST=1
36	50 G 0 DIPLEXER	NO_TEST=1
36	50 A 0 DIPLEXER	NO_TEST=1
36	50 G 1 DIPLEXER	NO_TEST=1
36	50 A 1 DIPLEXER	NO_TEST=1
36	50 G 2 DIPLEXER	NO_TEST=1
36	50 A 2 DIPLEXER	NO_TEST=1
36	50 0 COM	NO_TEST=1
36	50 0 ANT	NO_TEST=1
36	50 1 COM	NO_TEST=1
36	50 1 ANT	NO_TEST=1
36	50 2 COM	NO_TEST=1
36	50 2 ANT	NO_TEST=1

PCIE

35	PCH PCIE WLAN D2R C N	NO_TEST=1
35	PCH PCIE WLAN D2R C P	NO_TEST=1
35	PCH PCIE WLAN R2D N	NO_TEST=1
35	PCH PCIE WLAN R2D P	NO_TEST=1

BOM_COST_GROUP=PCB

H9M

PCIE

46 40	PCIE SOC R2D N<3..0>	NO_TEST=1
46 40	PCIE SOC R2D P<3..0>	NO_TEST=1
40	PCIE SOC D2R C N<3..0>	NO_TEST=1
40	PCIE SOC D2R C P<3..0>	NO_TEST=1

SSD PCIE

78 77 76 75 40	PCIE SSD0 D2R N<3..0>	NO_TEST=1
78 77 76 75 40	PCIE SSD0 D2R P<3..0>	NO_TEST=1
78 77 76 75 40	PCIE SSD0 R2D C N<3..0>	NO_TEST=1
78 77 76 75 40	PCIE SSD0 R2D C P<3..0>	NO_TEST=1

ESPI

38	ESPI IO R<3..0>	NO_TEST=1
113 38 12	ESPI IO<3..0>	NO_TEST=1
113 38 12	ESPI CLK	NO_TEST=1
12	ESPI CLK60M R	NO_TEST=1

XTAL

37	SOC XTAL24M OUT	NO_TEST=1
37	SOC XTAL24M IN	NO_TEST=1
37	SOC XTAL24M OUT R	NO_TEST=1

ENET

PCIE

81 80	PCIE ENET 1G D2R C N	NO_TEST=1
81 80	PCIE ENET 1G D2R C P	NO_TEST=1
81 80	PCIE ENET 1G R2D N	NO_TEST=1
81 80	PCIE ENET 1G R2D P	NO_TEST=1
84 82	PCIE ENET D2R C P<3..0>	NO_TEST=1
84 82	PCIE ENET D2R C N<3..0>	NO_TEST=1
84 82	PCIE ENET R2D N<3..0>	NO_TEST=1
84 82	PCIE ENET R2D P<3..0>	NO_TEST=1

MDI

85 80	ENETCONN MDI N<3..0>	NO_TEST=1
85 80	ENETCONN MDI P<3..0>	NO_TEST=1
85	ENET A N R	NO_TEST=1
85	ENET A P R	NO_TEST=1
85	ENET A CMC N	NO_TEST=1
85	ENET A CMC P	NO_TEST=1
107 85	ENET CONN A N	NO_TEST=1
107 85	ENET CONN A P	NO_TEST=1
85	ENET B N R	NO_TEST=1
85	ENET B P R	NO_TEST=1
85	ENET B CMC N	NO_TEST=1
85	ENET B CMC P	NO_TEST=1
107 85	ENET CONN B N	NO_TEST=1
107 85	ENET CONN B P	NO_TEST=1
85	ENET C N R	NO_TEST=1
85	ENET C P R	NO_TEST=1
85	ENET C CMC N	NO_TEST=1
85	ENET C CMC P	NO_TEST=1
107 85	ENET CONN C N	NO_TEST=1
107 85	ENET CONN C P	NO_TEST=1
85	ENET D N R	NO_TEST=1
85	ENET D P R	NO_TEST=1
85	ENET D CMC N	NO_TEST=1
85	ENET D CMC P	NO_TEST=1
107 85	ENET CONN D N	NO_TEST=1
107 85	ENET CONN D P	NO_TEST=1
85 82	ENET A N	NO_TEST=1
85 82	ENET A P	NO_TEST=1
85 82	ENET B N	NO_TEST=1
85 82	ENET B P	NO_TEST=1
85 82	ENET C N	NO_TEST=1
85 82	ENET C P	NO_TEST=1
85 82	ENET D N	NO_TEST=1
85 82	ENET D P	NO_TEST=1

PAGE TITLE
High speed No Testpoints

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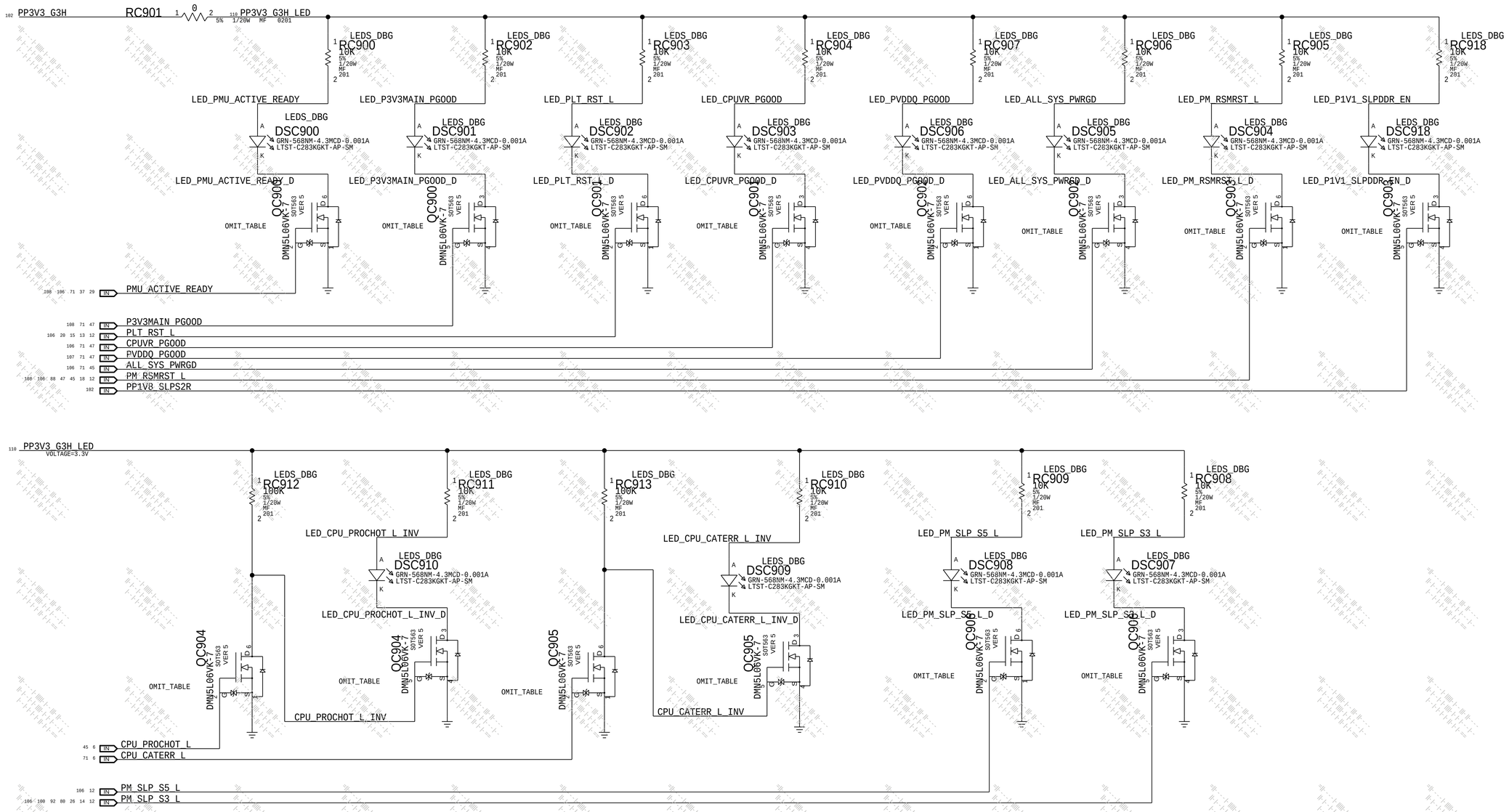

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	7	dual FET	QC900,QC901,QC902,QC903,QC904,QC905,QC906	CRITICAL	LEDS_DBG

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

DEBUG LEDS

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BOM_COST_GROUP=PCB

PAGE TITLE
Constraints

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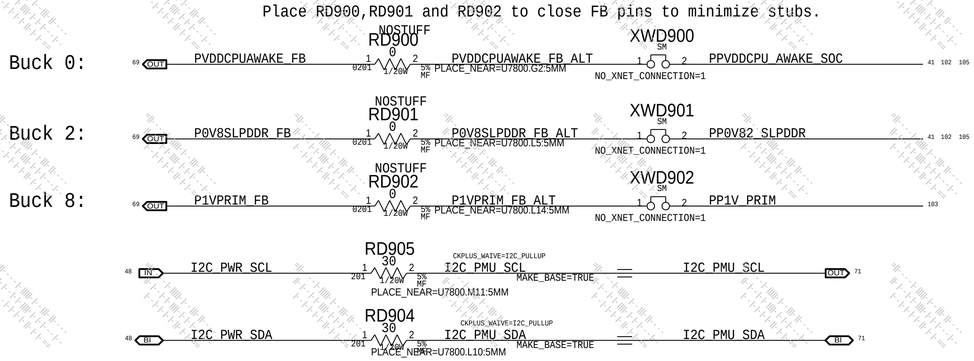
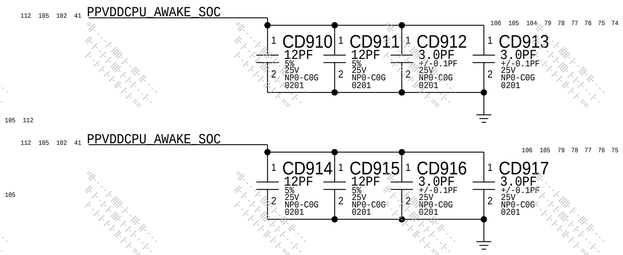
Calpe Dev Support:

Alternate Feedback:remote sense

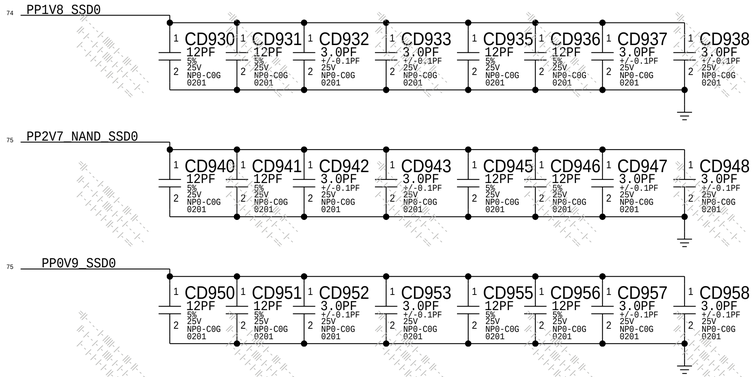
Place RD900,RD901 and RD902 to close FB pins to minimize stubs.



H9ML Desense Caps:



SSD/NAND Desense Caps:



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SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: Dev Support 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

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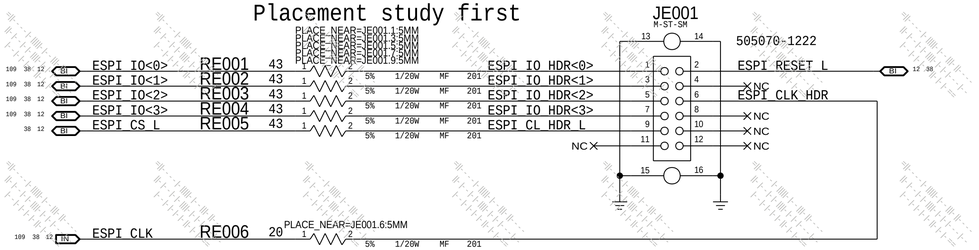
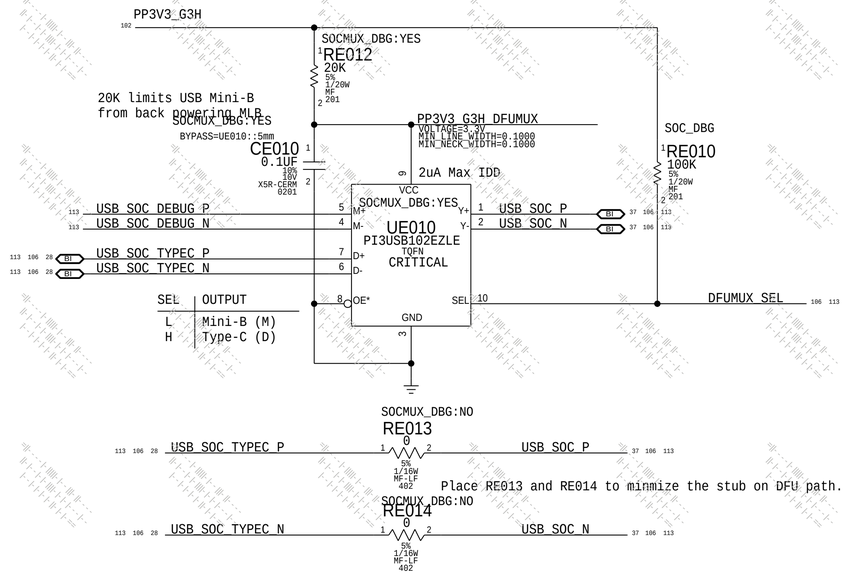
eSPI Analyzer

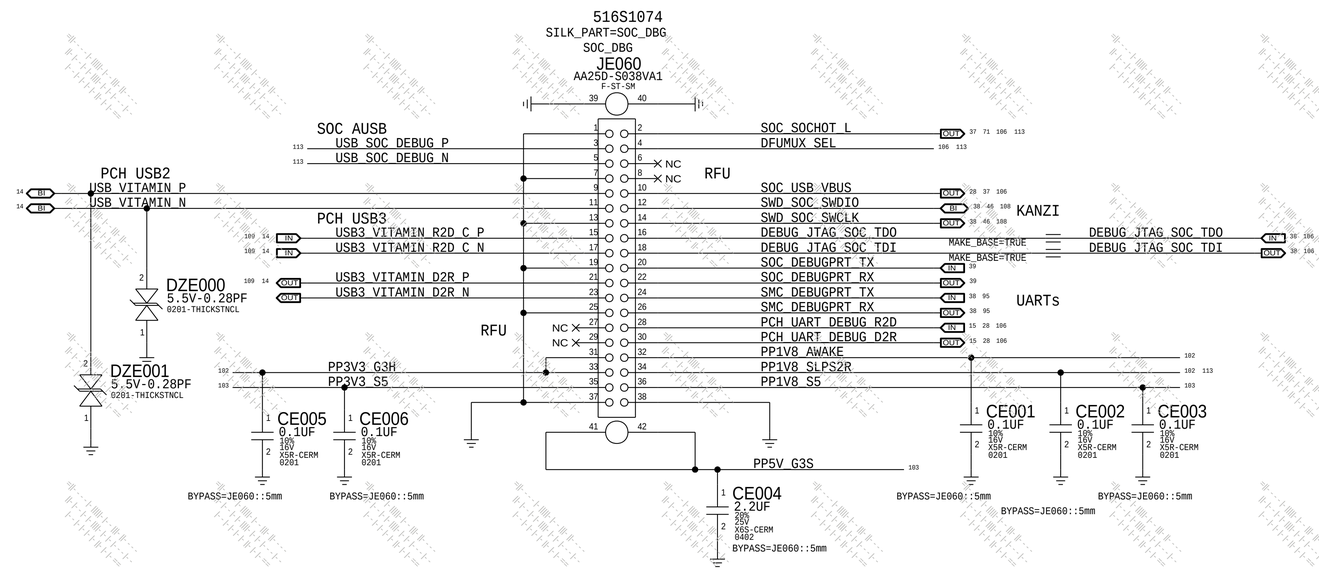
Placement study first



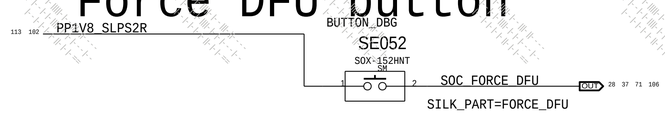
SoC USB DFU Mux



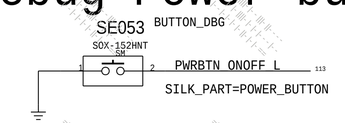
SOC DEBUG Connector

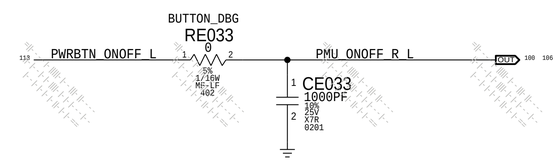


Force DFU button

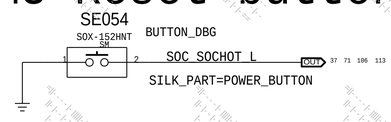


Debug Power button





PMU Reset button



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SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	Dev Support 2
Apple Inc.	DRAWING NUMBER 051-02424 / SIZE D
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BOM Variants

	BOM NUMBER	BOM NAME	BOM OPTIONS	
-->	639-06831	PCBA,MLB,3.6G_4C,X1036,128G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:128_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-06830	PCBA,MLB,3.6G_4C,X1036,128G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:128_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	3.6GHz 4C ENET_1G
	639-06849	PCBA,MLB,3.6G_4C,X1036,256G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06832	PCBA,MLB,3.6G_4C,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06833	PCBA,MLB,3.6G_4C,X1036,512G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06834	PCBA,MLB,3.6G_4C,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06835	PCBA,MLB,3.6G_4C,X1036,1TB_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06836	PCBA,MLB,3.6G_4C,X1036,1TB_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06837	PCBA,MLB,3.6G_4C,X1036,2TB_SM,ENET_1G	COMM_BOM,CPU:3.6G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
3.6GHz, ENET_10G->				
	639-06838	PCBA,MLB,3.6G_4C,X1036,128G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:128_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-06839	PCBA,MLB,3.6G_4C,X1036,128G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:128_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	3.6GHz 4C ENET_10G
	639-06840	PCBA,MLB,3.6G_4C,X1036,256G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06841	PCBA,MLB,3.6G_4C,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06842	PCBA,MLB,3.6G_4C,X1036,512G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06843	PCBA,MLB,3.6G_4C,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06844	PCBA,MLB,3.6G_4C,X1036,1TB_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06845	PCBA,MLB,3.6G_4C,X1036,1TB_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06846	PCBA,MLB,3.6G_4C,X1036,2TB_SM,ENET_10G	COMM_BOM,CPU:3.6G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
2.8GHz, ENET_1G->				
	639-05191	PCBA,MLB,2.8G,X1036,128G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:128_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-05383	PCBA,MLB,2.8G,X1036,128G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:128_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	2.8GHz 6C ENET_1G
	639-05177	PCBA,MLB,2.8G,X1036,256G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05385	PCBA,MLB,2.8G,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05387	PCBA,MLB,2.8G,X1036,512G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05391	PCBA,MLB,2.8G,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05393	PCBA,MLB,2.8G,X1036,1TB_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05397	PCBA,2.8G,MLB,X1036,1TB_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05959	PCBA,MLB,2.8GHz,X1036,2TB_SM,ENET_1G	COMM_BOM,CPU:2.8G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
2.8GHz, ENET_10G->				
	639-05189	PCBA,MLB,2.8G,X1036,128G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:128_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-05384	PCBA,MLB,2.8G,X1036,128G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:128_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	2.8GHz 6C ENET_10G
	639-05175	PCBA,MLB,2.8G,X1036,256G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05386	PCBA,MLB,2.8G,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05388	PCBA,MLB,2.8G,X1036,512G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05392	PCBA,MLB,2.8G,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05394	PCBA,MLB,2.8G,X1036,1TB_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05398	PCBA,2.8G,MLB,X1036,1TB_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05958	PCBA,MLB,2.8GHz,X1036,2TB_SM,ENET_10G	COMM_BOM,CPU:2.8G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
3.0GHz, ENET_1G->				
	639-05971	PCBA,MLB,3.0GHz,X1036,256G_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-05969	PCBA,MLB,3.0GHz,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	3.0GHz 6C ENET_1G
	639-05977	PCBA,MLB,3.0GHz,X1036,512G_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05975	PCBA,MLB,3.0GHz,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05983	PCBA,MLB,3.0GHz,X1036,1T_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05981	PCBA,MLB,3.0GHz,X1036,1T_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-05985	PCBA,MLB,3.0GHz,X1036,2T_SM,ENET_1G	COMM_BOM,CPU:3.0G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
3.0GHz, ENET_10G->				
	639-05968	PCBA,MLB,3.0GHz,X1036,256G_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-05966	PCBA,MLB,3.0GHz,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	3.0GHz 6C ENET_10G
	639-05974	PCBA,MLB,3.0GHz,X1036,512G_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05972	PCBA,MLB,3.0GHz,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05980	PCBA,MLB,3.0GHz,X1036,1T_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05978	PCBA,MLB,3.0GHz,X1036,1T_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05984	PCBA,MLB,3.0GHz,X1036,2T_SM,ENET_10G	COMM_BOM,CPU:3.0G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
3.2GHz, ENET_1G->				
	639-05997	PCBA,MLB,3.2GHz,X1036,256G_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
	639-05995	PCBA,MLB,3.2GHz,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	3.2GHz 6C ENET_1G
	639-06003	PCBA,MLB,3.2GHz,X1036,512G_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06001	PCBA,MLB,3.2GHz,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06009	PCBA,MLB,3.2GHz,X1036,1T_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06007	PCBA,MLB,3.2GHz,X1036,1T_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	
	639-06011	PCBA,MLB,3.2GHz,X1036,2T_SM,ENET_1G	COMM_BOM,CPU:3.2G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM	<-
3.2GHz, ENET_10G->				
	639-05994	PCBA,MLB,3.2GHz,X1036,256G_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-
	639-05992	PCBA,MLB,3.2GHz,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	3.3GHz 6C ENET_10G
	639-06000	PCBA,MLB,3.2GHz,X1036,512G_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-05998	PCBA,MLB,3.2GHz,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06006	PCBA,MLB,3.2GHz,X1036,1T_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06004	PCBA,MLB,3.2GHz,X1036,1T_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	
	639-06010	PCBA,MLB,3.2GHz,X1036,2T_SM,ENET_10G	COMM_BOM,CPU:3.2G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM	<-

Note:SSD SD and WD are the same

BOM_COST_GROUP=PCB

SYNC_MASTER:Mary SYNC_DATE:04/26/2018

PAGE TITLE: 639 BOM Configuration 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

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X1036 BOM Groups

BOM GROUP	BOM OPTIONS
X1036_COMMON_ALL	ALTERNATE,COMMON,X1036_COMMON1,X1036_COMMON2,X1036_COMMON3,X1036_DEFAULT
X1036_DEFAULT	SSD0_NAND_VCC:2.5V,ALL_SYS_PGD:1V8,SPIHOLD:H9M,CPUPEG:X8X4X4
X1036_COMMON1	X1036_PROGRAMMABLE:ENG,X1036_MODULE_PARTS:ENG,X1036_REV:DVT
X1036_COMMON2	X1036_HDMI,X1036_ID
X1036_COMMON3	LOADISNS,VR_BULKCAP:CURRENT,SENSOR:DEV,LOADRC:YES,ENGISNS:YES,XDP:YES
X1036_ENG:NO	FAN_DBG
X1036_ENG:YES	XDP_CONN,WIFI_DBG,USBC_DBG,SOC_DBG,SSD_DBG,LEDS_DBG,SOCMUX_DBG:YES,BUTTON_DBG
X1036_PROGRAMMABLE:ENG	TBT_T_ROM:DVT,TBT_X_ROM:DVT,BT_FLASH:DVT,WLAN_EEPROM:DVT,SOC_ROM:BLANK,SEPROM:OG,HDMI_ROM:DVT
X1036_MODULE_PARTS:ENG	PCH:PRQ,TBT_TR:C1,ACE:C0,PMU:A0_C,WIFI:ES7,HDMI:A4
X1036_HDMI	CLK_FILT,DATA_FILT,HDMI_RST:OD
X1036_ENET_10G	ENET:10G,10G_ENET:B1,10G_ENET_ROM:DVT,ENET_REFCLK:OSC
X1036_ENET_1G	ENET:1G,1G_ENET:A0,1G_ENET_ROM:DVT
X1036_ID	BOARDID1,BOARDID2,BOARDID3
X1036_REV:DVT	BOARDREV2,BOARDREV1,BOARDREV0
X1036_DEVEL:DVT	X1036_ENG:YES,ALTERNATE
X1036_DEV_1G_ENET	LED_1G_ENET_DBG,ALTERNATE
X1036_DEV_10G_ENET	DEBUG_LEDS:10G,ALTERNATE

COMMON BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00130	COMMON PARTS,MLB,X1036	X1036_COMMON_ALL

DEV BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00836	DEV(DEBUG)_COMMON PARTS,MLB,X1036	X1036_DEVEL:DVT
985-00853	1G ENET DEV/DEBUG PARTS,MLB,X1036	X1036_DEV_1G_ENET
985-00854	10G ENET DEV/DEBUG PARTS,MLB,X1036	X1036_DEV_10G_ENET

BOM VARIATION

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-00836	1	COMMON DEV/DEBUG,MLB,X1036	DEVEL	CRITICAL	DEV_BOM
685-00130	1	COMMON PARTS,MLB,X1036	COMM	CRITICAL	COMM_BOM
985-00853	1	1G ENET DEBUG,MLB,X1036	1G_DEVEL		1GDBG_BOM
985-00854	1	10G ENET DEBUG,MLB,X1036	10G_DEVEL		10GDBG_BOM

Alternatives section 2

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S00042	128S0329	ALL	CB200 etc rdr 37042037	
128S0311	128S0329	ALL	CB200 etc rdr 37042037	
353S00107	353S3239	ALL	U5400 erc rdr 37173893	
353S1429	353S3239	ALL	U5540 erc rdr 37175030	
107S00055	107S00090	ALL	U5540 erc rdr 37175230	
107S00056	107S00086	ALL	R5430 erc rdr 37175329	
107S0276	107S00020	ALL	R5600 erc rdr 37175569	
103S0321	103S0276	ALL	R5545 erc rdr 38515379	
138S0775	138S0860	ALL	C3198 etc rdr 38305368	
138S00049	138S0831	ALL	C8611 etc rdr 38306891	
311S00192	311S00191	ALL	U8312 etc rdr 37077481	
138S00024	138S0986	ALL	C3701/2/3 rdr 37399555	
103S00248	103S00247	ALL	R9000 rdr 38514938	
103S00250	103S00249	ALL	R9001/3 rdr 38515246	
128S0364	128S00081	ALL	C6482/3 rdr 37292870	
128S0264	128S00081	ALL	C6482/3 rdr 37292870	
377S00103	377S00138	ALL	DZB801/2 rdr 36419223	
377S0124	377S00138	ALL	DZB801/2 rdr 36419223	
138S00013	138S0772	ALL	C9921 rdr 38080947	ENET:10G
118S00093	118S00092	ALL	RA720 etc rdr 38513679	
138S0945	138S0706	ALL	C6360 etc rdr 38310616	
155S0387	155S0694	ALL	LA601 etc rdr 39358850	
155S00204	155S0731	ALL	FLA800 etc rdr 39359536	
138S00084	138S00060	ALL	C2950 etc rdr 38312295	
371S00085	371S00190	ALL	D3100 etc rdr 39225721	
138S00262	138S0806	ALL	C6000 rdr 39360099	

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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Apple Inc.

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